SGS-THOMSON MICROELECTRONICS

STLC7549

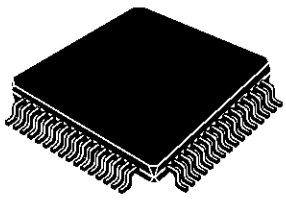
STEREO AUDIO/MODEM/TELEPHONY CODEC

ADVANCE DATA

- STEREO AUDIO CODEC WITH CD QUALITY NOISE AND DISTORTION
  - ADC AND DAC SAMPLING RATES UP TO 48kHz
  - 16-BIT RESOLUTION
  - > 85dB DYNAMIC RANGE
- QUADRAPHONIC MODE FOR SURROUND SOUND APPLICATION (STEREO AUDIO CODEC PLUS BOTH MONOPHONIC CODECS)
- MONOPHONIC CODEC FOR MODEM APPLICATIONS
  - ADC AND DAC SAMPLING RATES UP TO 44.1kHz
  - 16-BIT RESOLUTION
  - > 90dB DYNAMIC RANGE (MODEM MODE)
  - V.34 MODEM PERFORMANCE CAPABILITY
- SECOND MONOPHONIC CODEC FOR LOCAL HANDSET (or 2nd MODEM) APPLICATIONS
  - ADC AND DAC SAMPLING RATES UP TO 44.1kHz
  - 16-BIT RESOLUTION
  - > 85dB DYNAMIC RANGE (MODEM MODE)
- EXTENSIVE AUDIO SWITCHING AND GAIN CONTROLS FOR AUDIO ROUTING
  - A SUPERSET FEATURE LIST OF SOUNDBLASTER PRO AND MPC-2 SPECIFICATIONS
  - 3 STEREO LINE LEVEL INPUTS (LINE IN, CDROM, AUX)
  - 2 MONOPHONIC MICROPHONE INPUTS (DESKTOP AND HEADSET)
  - 2 PAIR OF STEREO OUTPUTS (MAIN AND AUXILLARY)
  - MONO INPUT AND MONOPHONIC OUTPUT
  - PROGRAMMABLE GAIN/ATTENUATION/ MUTE BLOCKS ON ALL INPUTS AND OUTPUTS
- MODEM CODEC HAS GAIN/ATTENUATION BLOCKS
  - INPUTS AND OUTPUTS CAN OPERATE IN A BALANCED OR UNBALANCED CONFIGURATION
  - DAC OUTPUT CAN OPTIONALLY BE USED AS REAR CHANNEL SOUND EFFECTS FOR GAMES
- 2nd MODEM CODEC HAS GAIN/ATTENUATION/ MUTE BLOCKS ON INPUT AND OUTPUT
  - ADC CAN SELECT HANDSET MOUTHPIECE OR DESKTOP/HEADSET MICROPHONE
  - DAC OUTPUT CAN OPTIONALLY BE USED AS REAR CHANNEL SOUND EFFECTS FOR GAMES
  - DAC OUTPUT CAN OPTIONALLY BE USED TO DRIVE THE HEADSET EARPIECE
  - THIS CODEC CAN ALSO BE USED FOR A SECOND MODEM PORT
- CONTROL PINS TO CONTROL LINE OUT ATTENUATORS BY PUSHBUTTONS UP/DOWN/MUTE
- CONTROL PIN TO CONTROL LINE OUT ATTENUATORS BY A DC-VOLTAGE POTENTIOMETER
- GENERAL PURPOSE DIGITAL I/O LINES FOR CONTROL OF MISCELLANEOUS TELEPHONE CIRCUITS
- EXTENSIVE POWER DOWN OPTIONS WITH LOW-POWER AUDIO LOOPTHRU MODE
- DUAL SYNCHRONOUS SERIAL PORTS WITH 64 BITS PER FRAME
- DIGITAL POWER SUPPLY OF 3.3V TO 5.0V
- ANALOG POWER SUPPLY OF 5V
- AVAILABLE IN 64 PIN TQFP PACKAGE

DESCRIPTION

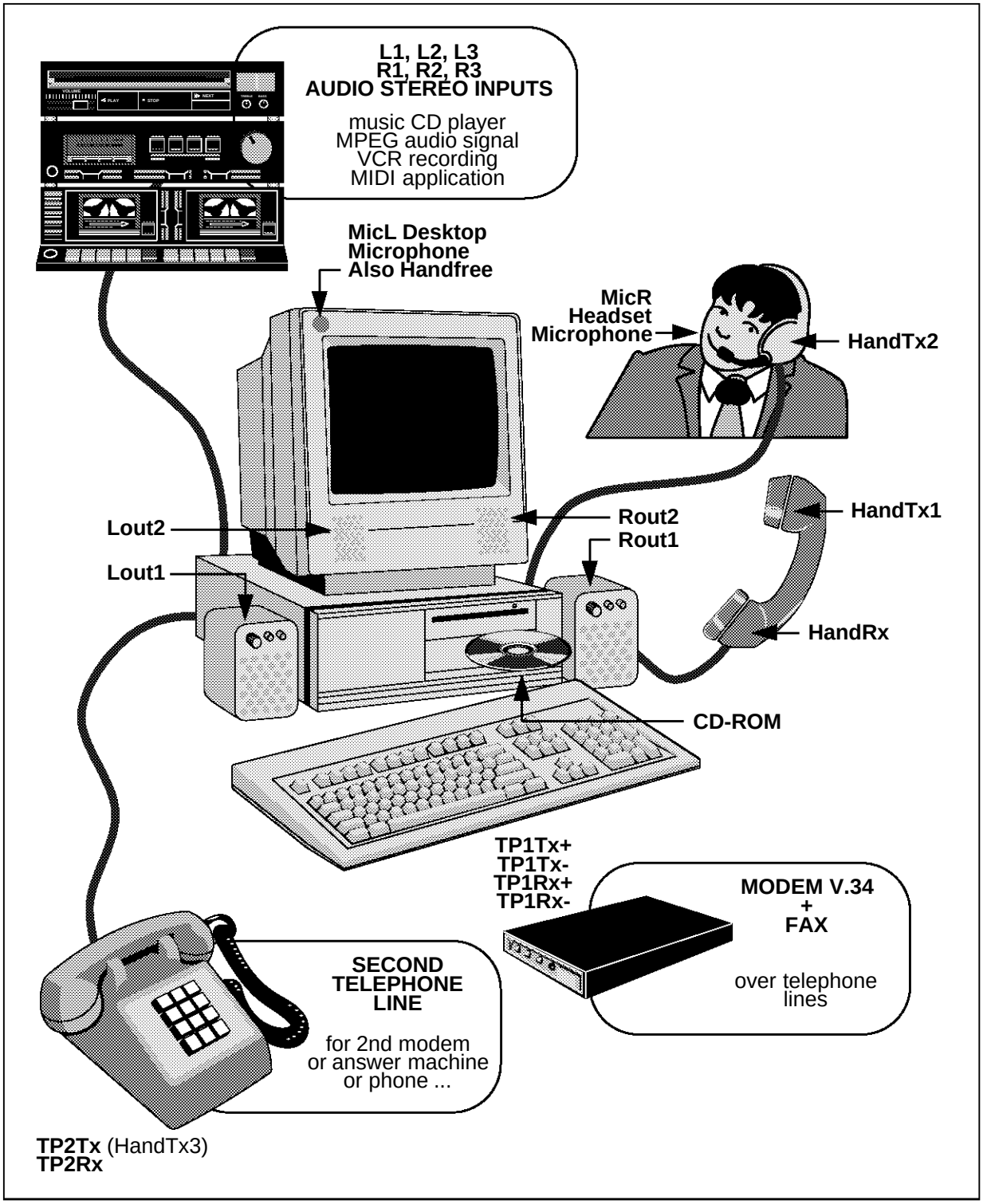
The STLC7549 codec is a single chip multimedia codec that contains multiple 16-bit sigma-delta codecs and a wide assortment of audio switching and gain controls.



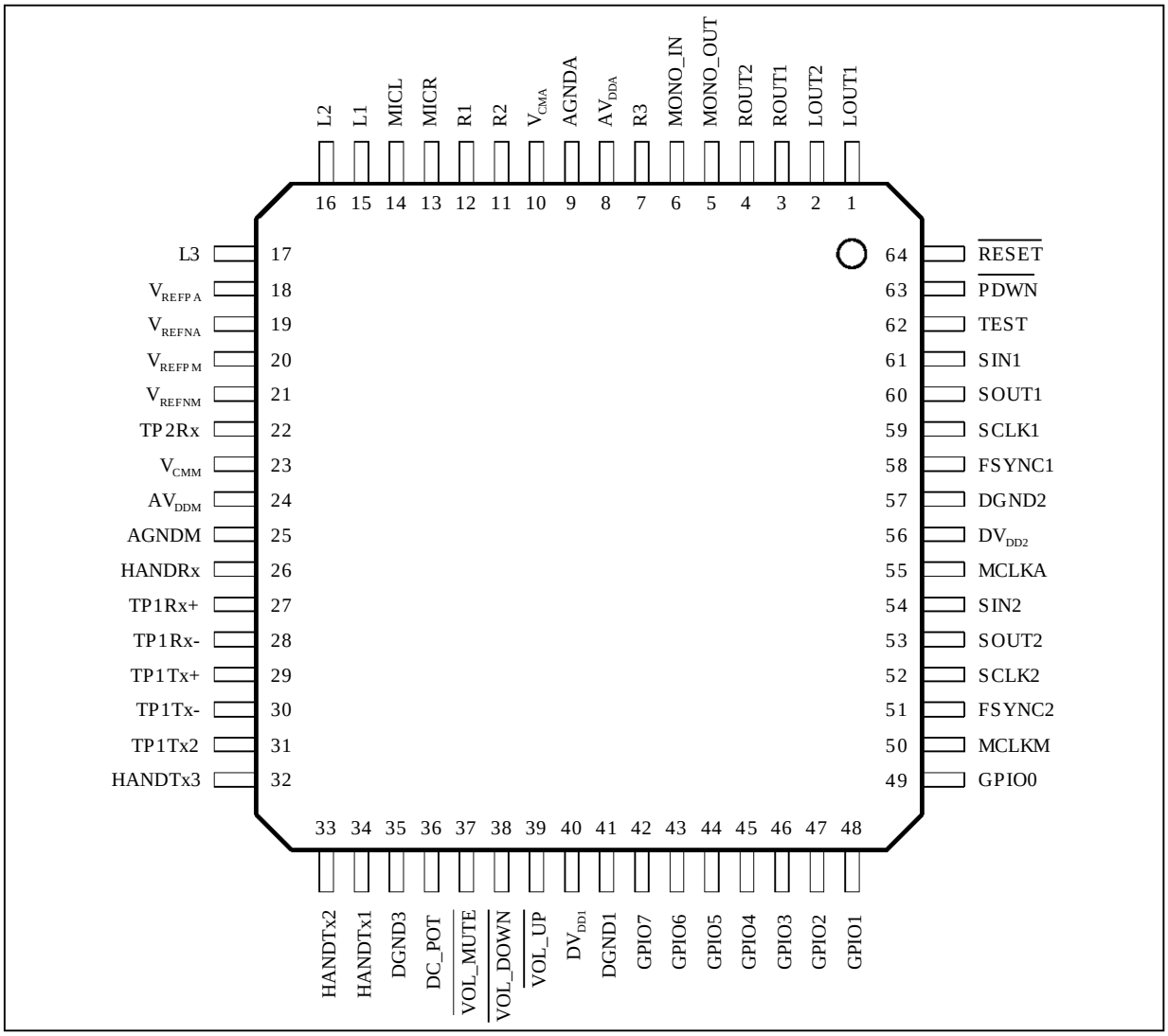
TQFP64
(Thin Quad Flat Pack)

ORDER CODE : STLC7549

MULTIMEDIA WORLD



PIN CONNECTIONS



PIN DESCRIPTION

Pin N°	Symbol	Type	Function
POWER SUPPLY (9 pins) (see Notes 1 and 2)			
8	AV_{DDA}	I	Analog V_{DD} Supply. This pin is the positive analog power supply voltage (4.75V to 5.25V) for the DAC and the ADC audio section. The voltage on these pins must be higher or equal to the voltage of the Digital power supply (DV_{DD}).
24	AV_{DDM}	I	Analog V_{DD} Supply. This pin is the positive analog power supply voltage (4.75V to 5.25V) for the DAC and the ADC modem and telephony section. The voltage on this pin must be higher or equal to the voltage of the Digital power supply (DV_{DD}).
40,56	DV_{DD1}, DV_{DD2}	I	Digital V_{DD} Supply. This pin is the positive digital power supply (3.15V to 5.25V).
9	AGNDA	I	Analog Ground. This pin is the ground return of the analog DAC (ADC) audio section.
25	AGNDM	I	Analog Ground. This pin is the ground return of the analog DAC (ADC) modem and telephony section.
41, 57, 35	DGND1, DGND2, DGND3	I	Digital Ground. These pins are the ground return of the digital section.

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Notes : 1. To obtain published performance, the analog V_{DD} and digital V_{DD} should be decoupled with respect to analog ground and digital ground, respectively. The decoupling is intended to isolate digital noise from the analog section ; decoupling capacitors should be as close as possible to the respective analog and digital supply pins (refer to Figure 11).

2. All the ground pins must be tied together. In the following section, the ground and supply pins are referred to as GND and V_{DD}, respectively.

PIN DESCRIPTION (continued)

Pin N°	Symbol	Type	Function
STEREO AUDIO CODEC (17 pins)			
Voltage Reference			
18	V_{REFPA}	O	Stereo Audio DAC and ADC Positive Reference Voltage Output. This pin provides the Positive Reference Voltage used by the 16-bit stereo audio converters. The reference voltage, V_{REFA}, is the voltage difference between the V_{REFPA} and V_{REFNA} outputs. V_{REFPA} should be externally decoupled with respect to V_{CMA}. $V_{REFA} = V_{REFPA} - V_{REFNA}$.
19	V_{REFNA}	O	Stereo Audio DAC and ADC Negative Reference Voltage Output. This pin provides the Negative Reference Voltage used by the 16-bit stereo audio converters, and should be externally decoupled with respect to V_{CMA}.
10	V_{CMA}	O	Audio Common Mode Voltage Output. This output pin is the common mode voltage (AV_{DDA}-AGNDA)/2. This output must be decoupled with respect to AGNDA.
Analog Inputs			
15	L1	I	Left Line Input #1. Left analog input #1. Full scale input, with no gain, is $1V_{RMS}$, centered at V_{CMA}.
16	L2	I	Left Line Input #2. Left analog input #2. Full scale input, with no gain, is $1V_{RMS}$, centered at V_{CMA}.
17	L3	I	Left Line Input #3. Left analog input #3. Full scale input, with no gain, is $1V_{RMS}$, centered at V_{CMA}.
14	MICL	I	Left Microphone Input. Microphone input for the left MIC channel, centered at V_{CMA}. This signal can be either $1V_{RMS}$ or $0.1V_{RMS}$ depending on the preamp gain.
12	R1	I	Right Line Input #1. Right analog input #1. Full scale input, with no gain, is $1V_{RMS}$, centered at V_{CMA}.
11	R2	I	Right Line Input #2. Right analog input #2. Full scale input, with no gain, is $1V_{RMS}$, centered at V_{CMA}.
7	R3	I	Right Line Input #3. Right analog input #3. Full scale input, with no gain, is $1V_{RMS}$, centered at V_{CMA}.
13	MICR	I	Right Microphone Input. Microphone input for the right MIC channel, centered at V_{CMA}. This signal can be either $1V_{RMS}$ or $0.1V_{RMS}$ depending on the preamp gain.
6	MONO_IN	I	Monophonic input , centered at V_{CMA}. This signal can be $1V_{RMS}$. This is a general purpose mono analog input that is normally used to mix the typical "beeper" signal on most computers into the audio system.
Analog Outputs			
1	LOUT1	O	Left Channel Output #1. Left channel analog output. Maximum signal is $1V_{RMS}$ centered at V_{CMA}.
2	LOUT2	O	Left Channel Output #2. Left channel analog output. Maximum signal is $1V_{RMS}$ centered at V_{CMA}.
3	ROUT1	O	Right Channel Output #1. Right channel analog output. Maximum signal is $1V_{RMS}$ centered at V_{CMA}.
4	ROUT2	O	Right Channel Output #2. Right channel analog output. Maximum signal is $1V_{RMS}$ centered at V_{CMA}.
5	MONO_OUT	O	Mono Output. This output is a summed analog output from the left and right and Mono input channels. Maximum signal is $1V_{RMS}$ centered at V_{CMA}.
MODEM AND TELEPHONY CODEC (13 pins)			
20	V_{REFPM}	O	Modem and Telephony DAC and ADC Positive Reference Voltage Output. This pin provides the Positive Reference Voltage used by the 16-bit modem converters and the 16-bits telephony converters. The reference voltage, V_{REFM}, is the voltage difference between the V_{REFPM} and V_{REFNM} outputs. V_{REFPM} should be externally decoupled with respect to V_{CMM}. $V_{REFM} = V_{REFPM} - V_{REFNM}$.
21	V_{REFNM}	O	Modem and Telephony DAC and ADC Negative Reference Voltage Output. This pin provides the Negative Reference Voltage used by the 16-bit modem converters and the 16-bits telephony converters, and should be externally decoupled with respect to V_{CMM}.
23	V_{CMM}	O	Modem and Telephony Common Mode Voltage Output. This output pin is the common mode voltage (AV_{DDM}-AGNDM)/2. This output must be decoupled with respect to GND.

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PIN DESCRIPTION (continued)

Pin N°	Symbol	Type	Function
MODEM AND TELEPHONY CODEC (13 pins) (continued)			
29	TP1Tx+	O	Modem #1 Differential Positive Output. This pin is the noninverting output of the fully differential transmit output modem #1.
30	TP1Tx-	O	Modem #1 Differential Negative Output. This pin is the inverting output of the fully differential transmit output modem #1. Outputs TP1Tx+ and TP1Tx- provide analog signals with maximum peak-to-peak amplitude 2 x V_{REFM}, and must be followed by an external two pole smoothing filter. The external filter follows the internal single pole switch capacitor filter with cut-off frequency of 2 x FSM. The cut-off frequency of the external filter must be greater than two times the sampling frequency (FSM), so that the combined frequency response of both the internal and external filters is flat in the band-pass.
27	TP1Rx+	I	Modem #1 Differential Positive Analog Input. This pin is the differential non-inverting ADC input.
28	TP1Rx-	I	Modem #1 Differential Negative Analog Input. This pin is the differential inverting receive input. The analog input peak-to-peak differential signal range must be less than 2 x V_{REFM}, and must be preceeded by an external single pole anti-aliasing filter. The cut-off frequency of the filter must be lower than one half the over-sampling frequency. These filters should be set as close as possible to the TP1Rx+ (TP1Rx-) pins.
31	TP1Tx2 (LQ1)	O	Modem #1 Auxiliary Analog Output or left channel output in quadraphonic mode (LQ1). This pin is the single-ended auxillary modem output. This output provides analog signals with maximum peak-to-peak amplitude V_{REFM}, and must be followed by an external two pole smoothing filter. The external filter follows the internal single pole switch capacitor filter. The cut-off frequency of the external filter must be greater than two times the sampling frequency (FSM), so that the combined frequency response of both the internal and external filters is flat in the band-pass.
34 33 32	HandTx1, HandTx2, HandTx3 (TP2Tx) (RQ1)	O	Telephony Single-ended Outputs or right channel output in quadraphonic mode for TP2Tx (RQ1). These pins are the single-ended outputs of the analog smoothing filter. With maximum peak-to-peak amplitude V_{REFM}, and must be followed by an external two pole smoothing filter. The external filter follows the internal single pole switch capacitor filter. The cut-off frequency of the external filter must be greater than two times the sampling frequency (FSM), so that the combined frequency response of both the internal and external filters is flat in the band-pass.
26 22	HandRx TP2Rx	I	Telephony Single-ended Input. These pins are the single-ended Telephony ADC input. The analog input peak-to-peak single-ended signal range must be less than V_{REFM}, and must be preceeded by an external single pole anti-aliasing filter. The cut-off frequency of the filter must be lower than one half the over-sampling frequency. These filters should be set as close as possible to the TP2Rx, HandRx pins.
HOST INTERFACE (25 pins)			
Serial Interface #1 Dedicated for Stereo Audio Codec. The serial audio interface is synchronous with the audio sampling frequency (FSA).			
61	SIN1	I	Data In. Digital audio data to the DACs, control information, GPIO data are received by the STLC7549 via SIN1. Refer to "Serial Interface Bit Definition" on Page 21.
60	SOUT1	O	Data Out. Digital audio data from the ADCs, status information, GPIO data are output from the STLC7549 via SOUT1. Refer to "Serial Interface Bit Definition" on Page 21.
59	SCLK1	O	Serial Port #1 Bit Clock Output. Clocks the digital data into SIN1 and out of SOUT1 during the frame synchronization interval. The Serial bit clock is generated internally and is equal to the audio Master clock signal frequency MCLKA/(4 x N) where N depends on index register 20 contents.
58	FSYNC1	O	Serial Port #1 Frame Synchronization Output. The frame synchronization signal is used to indicate that the device is ready to send and receive data. The data transfer begins on the falling edge of the frame-sync signal. The frame-sync is generated internally and goes low on the rising edge of SCLK1. FSYNC1 and FSA have the same frequency.
55	MCLKA	I	Master Clock A for Audio Codec. Master clock input for audio codecs. This signal is the oversampling clock of the DA and AD convertor. It also provides all the clocks of the audio serial interface #1. This input must be driven by a signal with a frequency from 6.144MHz to 12.288MHz. In quadraphonic mode this input provide all Codecs clocks of the STLC7549.

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PIN DESCRIPTION (continued)

Pin N°	Symbol	Type	Function
HOST INTERFACE (25 pins) (continued)			
Serial Interface #2 Dedicated for Modem and Telephony Codecs. The serial modem interface is synchronous with the modem sampling frequency (FSM).			
54	SIN2	I	Data Input. Digital modem and telephony data to the DACs are received by the STLC7549 via SIN2.
53	SOUT2	O	Data Output. Digital modem and telephony data from the ADCs are output from the STLC7549 via SOUT2.
52	SCLK2	O	Serial Port #2 Bit Clock Output. Clocks the digital data into SIN2 and out of SOUT2 during the frame synchronization interval. The Serial bit clock is generated internally and equal to the Master clock signal frequency MCLKM/4. In quadraphonic mode SCLK2 is equal to MCLKA/4 (refer to Figure 4).
51	FSYNC2	O	Serial Port #2 Frame Synchronization Output. The frame synchronization signal is used to indicate that the device is ready to send and receive data. The data transfer begins on the falling edge of the frame-sync signal. The frame-sync is generated internally and goes low on the rising edge of SCLK2. FSYNC2 and FSM have the same frequency.
50	MCLKM	I	Master Clock M for Modem and Telephony Codecs. Master clock input for modem codecs. In quadraphonic mode this input is ignored. This signal is the oversampling clock of the DA and AD convertor. It also provides all the clocks of the modem serial interface #2. This input may be driven by a signal with a frequency from 1.8432MHz to 3.84MHz (up to 11.2896MHz in Quadraphonic mode).
Miscellaneous			
64	$\overline{\text{RESET}}$	I	Reset Function (active low). A reset function to initalize the internal counters and control register. A minimum low pulse of 100ns is required to reset the chip. This reset function initiates the serial data communications. The reset function will initialize all the registers to their default value and will put the device in a pre-programmed state. Master clocks are not necessary during RESET .
63	$\overline{\text{PDWN}}$	I	Power Down (active low). The Power-Down input powers down the entire chip to 0.5mW. When PDWN pin is taken low, the device is powered down such that the existing internally programmed state is maintained and all analog outputs are in high impedance. When PDWN is driven high, full operation resumes. If the PDWN input is not used, it should be tied to V_{DD}.
62	TEST	I	Test Input. Digital input reserved for test. Should be connected to GND.
39	$\overline{\text{VOL\_UP}}$	I	Pushbutton Lineout Control Volume UP (edge sensitive, active low, internal pull-up). This pin increases the volume and also affects the left and right gain select values in register 10.
38	$\overline{\text{VOL\_DOWN}}$	I	Pushbutton Lineout Control Volume DOWN (edge sensitive, active low, internal pull-up). This pin decreases the volume and also affects the left and right gain select values in the register 10.
37	$\overline{\text{VOL\_MUTE}}$	I	Pushbuttons Lineout Control Volume MUTE (edge sensitive, active low, internal pull-up). This pin mutes and unmutes (toggle function) the Left and Right attenuators overriding the mute bits in registers 11 and 12 (refer to Figure 8).
36	DC_POT	I	DC Potentiometer Control Lineout Volume. An external potentiometer can be attached to this pin to determine a 4-bit value to be used as the main Left/Right output attenuator register value (register 10).
49 : 42	GPIO[0:7]	I/O	General Purpose I/Os. General purpose input/output pins. These I/Os are configured as inputs at power-up or RESET.

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BLOCK DIAGRAM

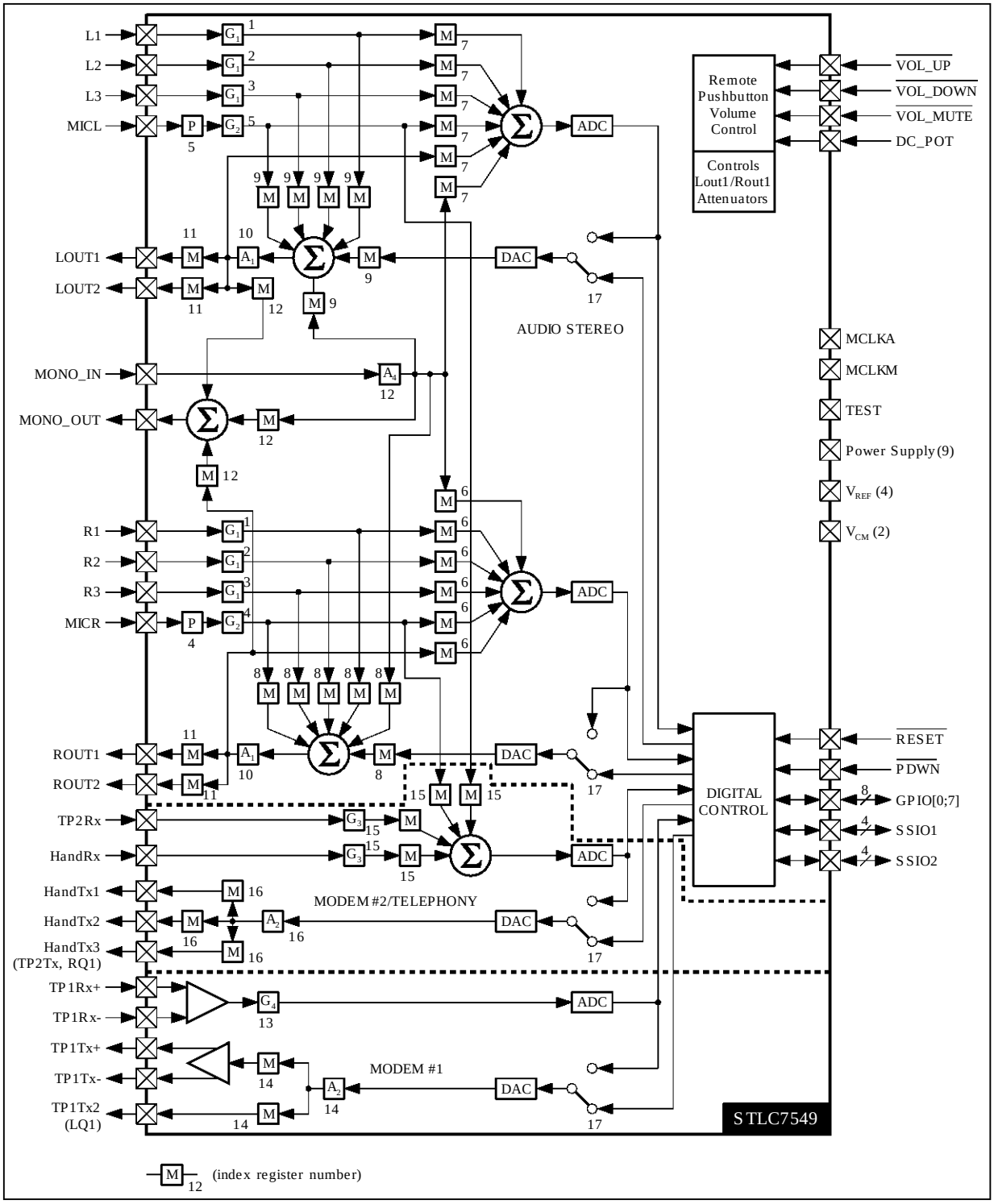


Figure 1 : Simplified Stereo Part Diagram

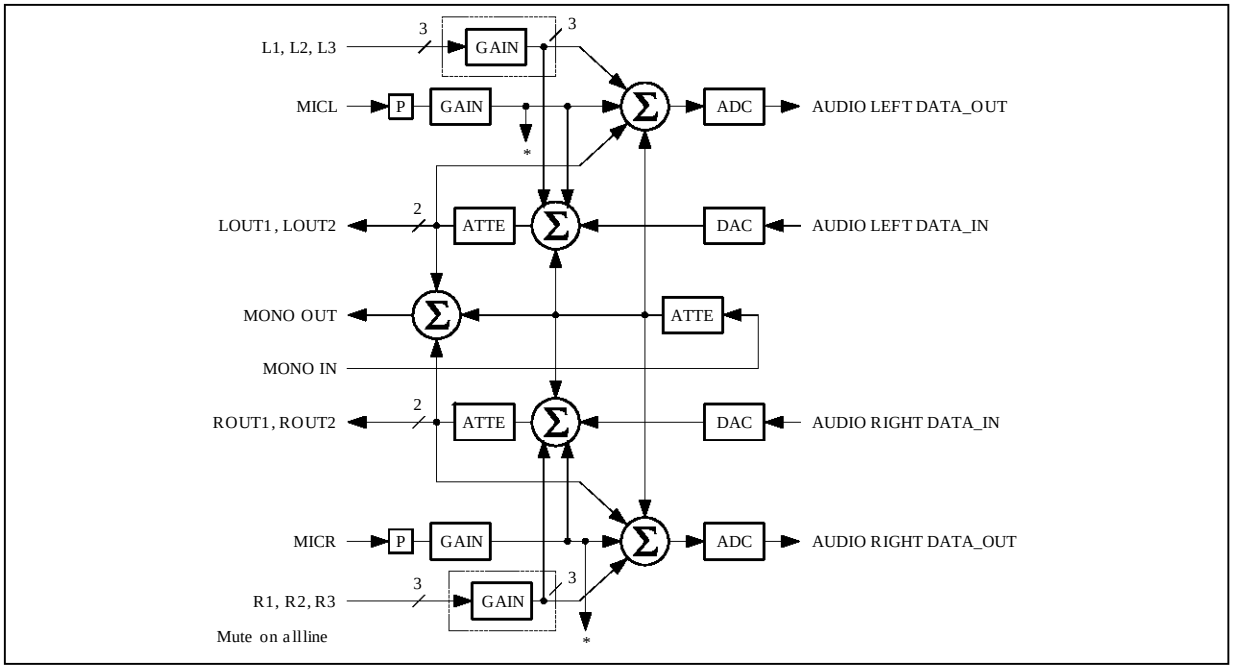


Figure 2 : Simplified Telephony/Modem #2 Part Diagram

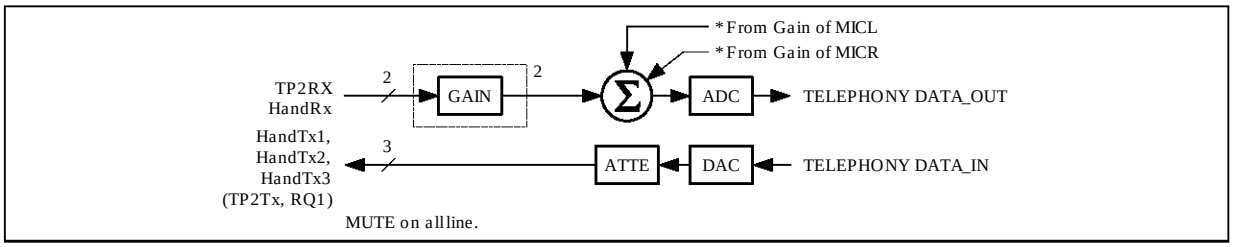


Figure 3 : Simplified Modem #1 Part Diagram

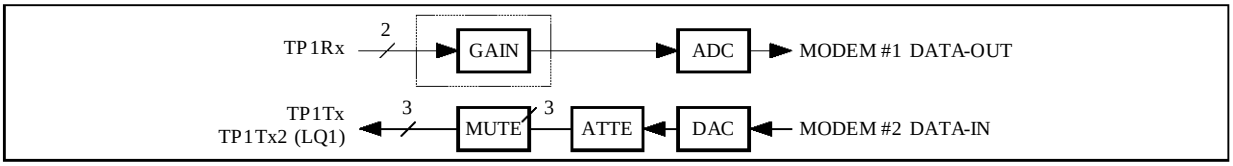
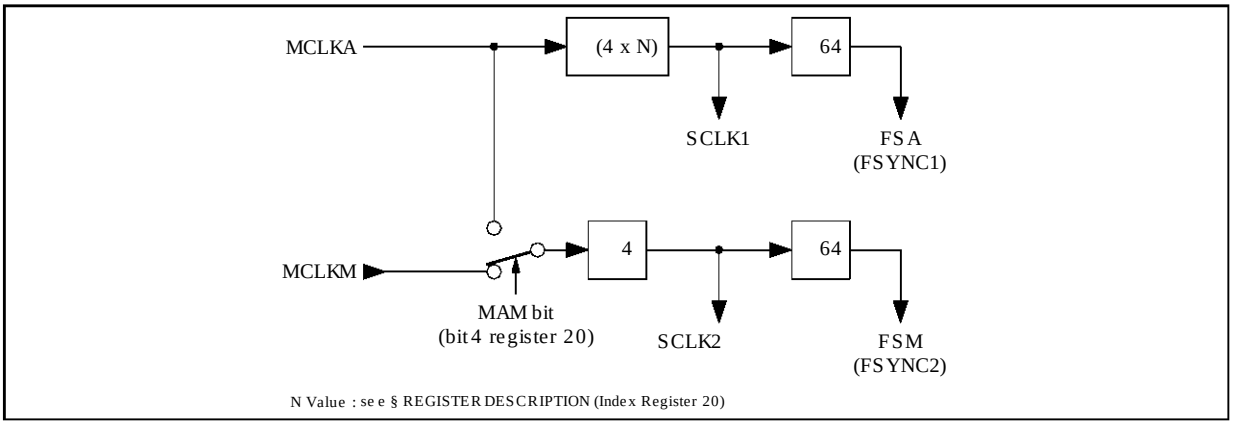


Figure 4 : Clock Generator Diagram



FUNCTIONAL DESCRIPTION

1 - Volume Control

The STLC7549 provides a powerful set of volume control functions via pushbuttons (VOL_MUTE, VOL_DOWN and VOL_UP input pins), a potentiometer (DC_POT input pin) and control registers (Register 10 : Audio line output attenuator control, Register 11 : Audio output mute control , Register 12 : Mono input/output control, Register 19 : digital control Register #1).

1.1 - Index Register 19 : Digital Control Register #1 Description

By setting the bits +PBVOL (pushbutton volume circuitry) or + DCVOL (DC volume control circuitry) the output attenuators will be affected (increment or decrement by 1 LSB the current 4-bit value of volume control Register 10) by the pushbuttons (VOL_UP ,VOL_DOWN) or by the potentiometer (DC voltage range pin DC_POT to determine a 4-bit value).

The 4-bit value from the DC potentiometer can be read from Register 19 (bits 4 to 7). If the bits +PBVOL and +DCVOL are both set to "1" the priority is given to +DCVOL.

In pushbutton mode the serial interface is still able to modify the volume setting of Register 10. In potentiometer mode the serial interface can not modify Register 10.

Index Register 19		Control Mode	
+PBVOL	**+DCVOL**	**VOLUME (1)**	**MUTE (2)**
0	0	Serial Interface	Serial Interface
1	0	Pushbuttons/ Serial Interface	Pushbuttons/ Serial Interface
0	1	Potentiometer	Serial Interface
1	1	Potentiometer	Pushbuttons

Notes : 1. Register 10
2. Registers 11,12

1.2 - Pushbuttons Circuitry

The pushbuttons volume circuitry (VOL_MUTE, VOL_UP and VOL_DOWN) will affect the main left/right output attenuator in Register 10 and mute blocks in Registers 11,12 and do not mute the PC speaker (Register 12). When switching from serial interface control mode to pushbuttons control mode the contents of the Registers 10,11,12 are kept. If more than 1 pushbutton is pushed, then the priority is given to the one pushed first.

The action on VOL_UP and VOL_DOWN pushbuttons will increment or decrement the contents of the left and right output attenuator in Register 10.The status of the input pins are inverted and reflected in bits 21, 22 and 23 of the serial output#1 interface. The input pins are debounced before acting on registers value. The input pins are edge sensitive and active low.

The push-buttons are debounced as shown in Figures 5 and 6. The internal pull-up resistance is over 20kΩ.

Figure 5

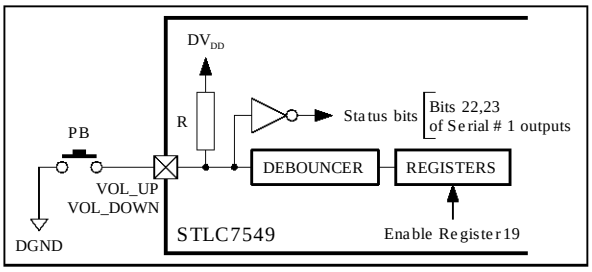
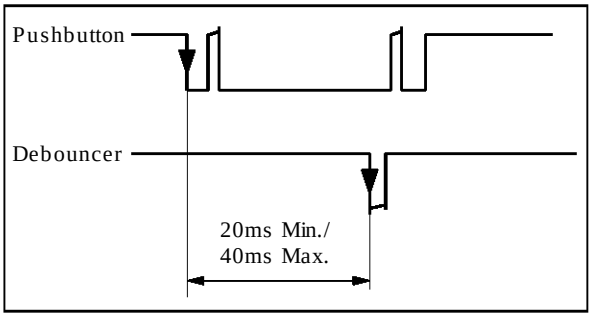


Figure 6

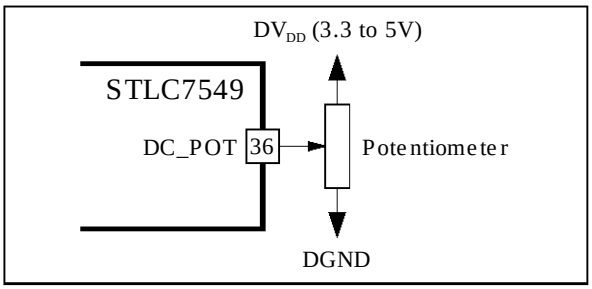


In order to better understand the MUTE pushbutton function please see Figure 8. After RESET the output of the TOGGLE/UNTOGGLE circuitry is in unmute position.

1.3 - Potentiometer circuitry

With the internal DC to 4-bit value convertor you can control the output volume just with a simple potentiometer of 100kΩ . When switched to DC volume control mode , the contents of the volume Register 10 are up-dated with the 4-bit convertor value of the potentiometer circuitry. The 4-bit value volume control register is up-dated at least every 100ms .The potentiometer circuitry has an hysteresis of 1/2 LSB. The DC potentiometer circuitry is shown in Figure 7.

Figure 7



FUNCTIONAL DESCRIPTION (continued)

2 - Mute Function

The mute function allows each input and output channel to be silenced independently. This function maintains the configuration (gain, attenuation, mixing configuration) during the mute and unmute. The output channels should be muted when the sampling frequency is changed.

For the complete description of the mute possibilities see :

- Register 6 (Right ADC Summer control)
- Register 7 (Left ADC Summer control)
- Register 8 (Right DAC Summer control)
- Register 9 (Left DAC Summer control)
- Register 11 (Audio output Mute control)
- Register 12 (Mono Input/Output control)
- Register 14 (Mono codec#1 output control)
- Register 15 (Mono codec#2 input control)
- Register 16 (Mono codec#2 output control)

3 - Input Gain and Output Gain Setting

Both input and output gain setting are internally made on zero crossing of the analog signal to minimize the " zipper " noise. The gain setting on zero crossing of the analog signal is not available in the preamplifier P. The gain change automatically takes effect if zero crossing does not occur within 512 frames. The 512 frames counter is initialized by the register gain access.

4 - Offset Cancellation

The internal input offsets are minimized by internal offset cancellation circuitry . The calibration procedure is forced by setting bit 0 or bit 1 of Register 19 to "1". The lengh of time required for calibration is 1024 samples at the sampling frequency rate (eg: FSx = 44.1kHz, T = 1024 * 1/FSx = 23ms). When calibration is completed the bit 0 or bit 1 of Register 19 is reset to "0". During calibration the analog inputs are set to a high impedance state and the data value at SOUT are not valid.

5 - Quadraphonic Mode

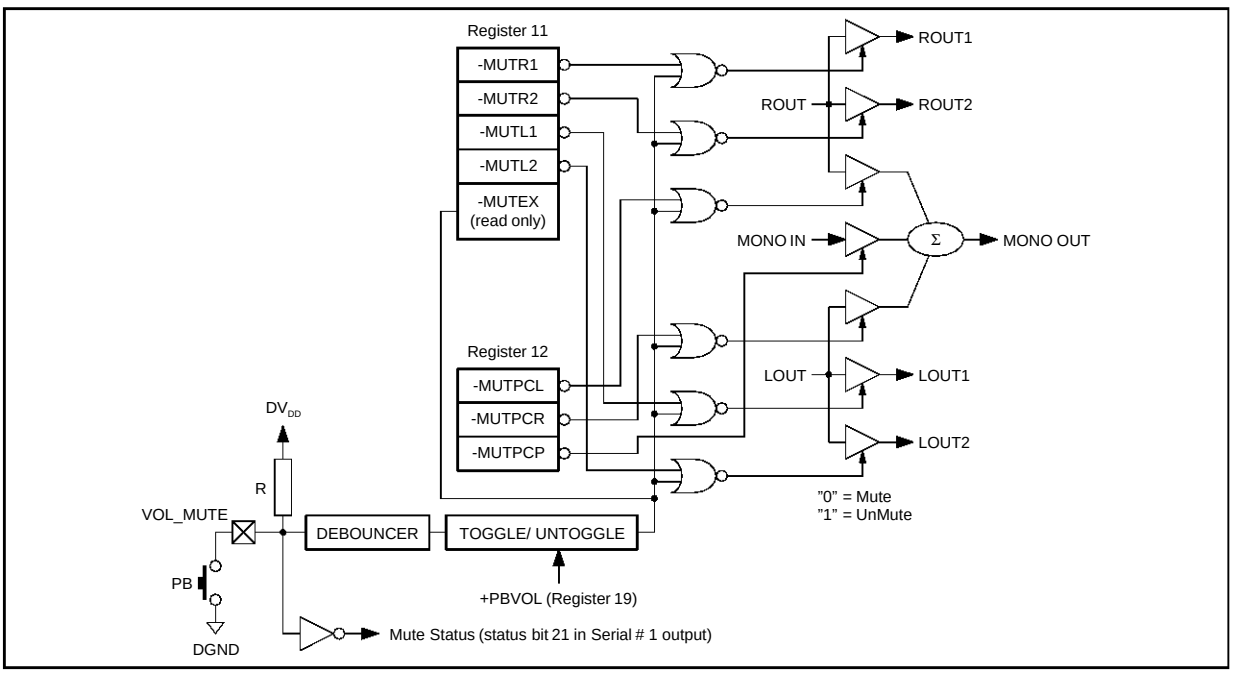
The STLC7549 offers the possibility to play music in quadraphonic mode. This mode will allow you to power your multimedia application by providing surround sound using RQ1 (Right Quadraphonic 1 output) and LQ1 (Left Quadraphonic 1 output) along with the normal stereo outputs Lout1 and Rout1.

This mode is programmed by setting the bit MAM (Modem Audio Mode, Register 20) to "1", this will cause the modem codecs #1 and #2 clocks to be controlled from the audio master clock MCLKA (11.2896MHz). The modem master clock MCLKM will be ignored (see CLOCK GENERATOR DIAGRAM) (Figure 4).

In this mode the FSA must be programmed to 44.1kHz (NDIV1 and NDIV0 of Register 20 equals zero so N=1). FSM will be equal to MCLKA/4/64 = 44.1kHz.

For Quadraphonic mode you will have also to program the bit MOR (Modem Oversampling Ratio, Register 20) to "1" so the oversampling ratio will be 128.

Figure 8 : Mute Function

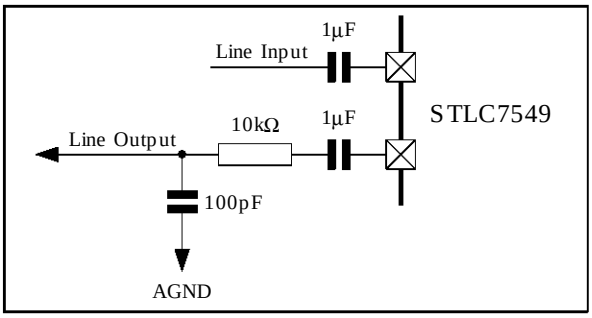


FUNCTIONAL DESCRIPTION (continued)

6 - Analog Inputs and Outputs

Figure 9 illustrates the suggested connection to obtain full performance from the STLC7549.
Any unused analog input should be tied to V_{CM} directly.

Figure 9

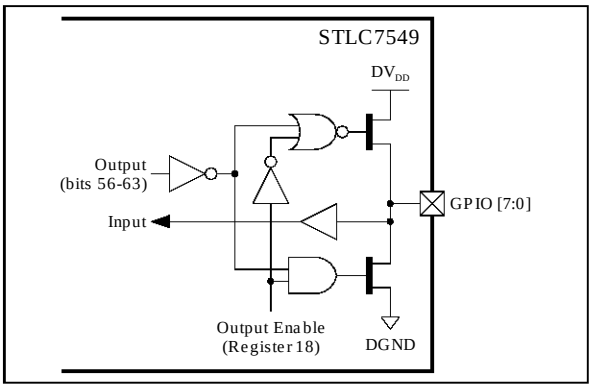


7 - General Purpose Input/Output : GPIO [7:0]

The STLC7549 offers 8 general purpose Input/Output pins.The setting of the GPIO configuration is done through Register 18 (bit set to "0" for input configuration and bit set to "1" for output configuration). On RESET the pins are configured as Input.

The GPIO value is reflected in the serial data stream SOUT1 bits 24-31 (eg : could be used for Ring detect in modem application). When programmed as output the GPIO provides the way to control external devices using bits in the serial data input stream SIN1 bits 56-63 (eg: could be used for controlling relay drivers) .The GPIO input voltage is independant of DV_{DD} and can be from 3.3V to 5V.

Figure 10



8 - Clock Generator

From the Master Clock Audio (MCLKA) and Master Clock Modem (MCLKM) the internal clock generator provides all the synchronous serial interface clocks (SCLK1, FSYNC1, SCLK2 and FSYNC2).

The internal sampling frequency (FSA , FSM) used for A/D and D/A conversion are equal to the synchronous frequency (FSYNC1 and FSYNC2 respectively) . FSx and FSYNCx frequencies are not in phase.

In Quadraphonic mode the MCLKM input is ignored and the reference master clock is MCLKA. For proper operation the N divider (Register 20) must be set to 1 in order to have FSA and FSM equals.

The modem codecs can run with master clock higher than 3.84MHz (e.g. : 11.2896MHz) but with reduced performances.

9 - Reset and Power Down

The reset function initializes the internal counters and control registers. A minimum low pulse of 100ns is required to reset the chip. This reset function initiates the serial data communication. During reset operation the SCLKx, FSYNCx and SOUTx output are driven high.

After a reset :

- the registers are set to a known value (refer to register description)
- the GPIO [0:7] are set to Input configuration.
- the output of TOGGLE/UNTOGGLE mute function is placed in unmute state.
- all the internal data paths are set to " 0 ".
- the calibrations of all converters are lost.

The $\overline{PDWN}$ input powers down the entire chip. Minimum power consumption is obtained when the MCLKx are stopped. When $\overline{PDWN}$ pin is taken low the device powers down such that the existing programmed state is maintained and all analog outputs are in a high impedance state. In power down mode the Vcmx is floating. When power down is driven high full operation resumes. If the power down input is not used, it should be tied to DV_{DD}.

The STLC7549 provides also 3 software power down modes detailed in Register 20.

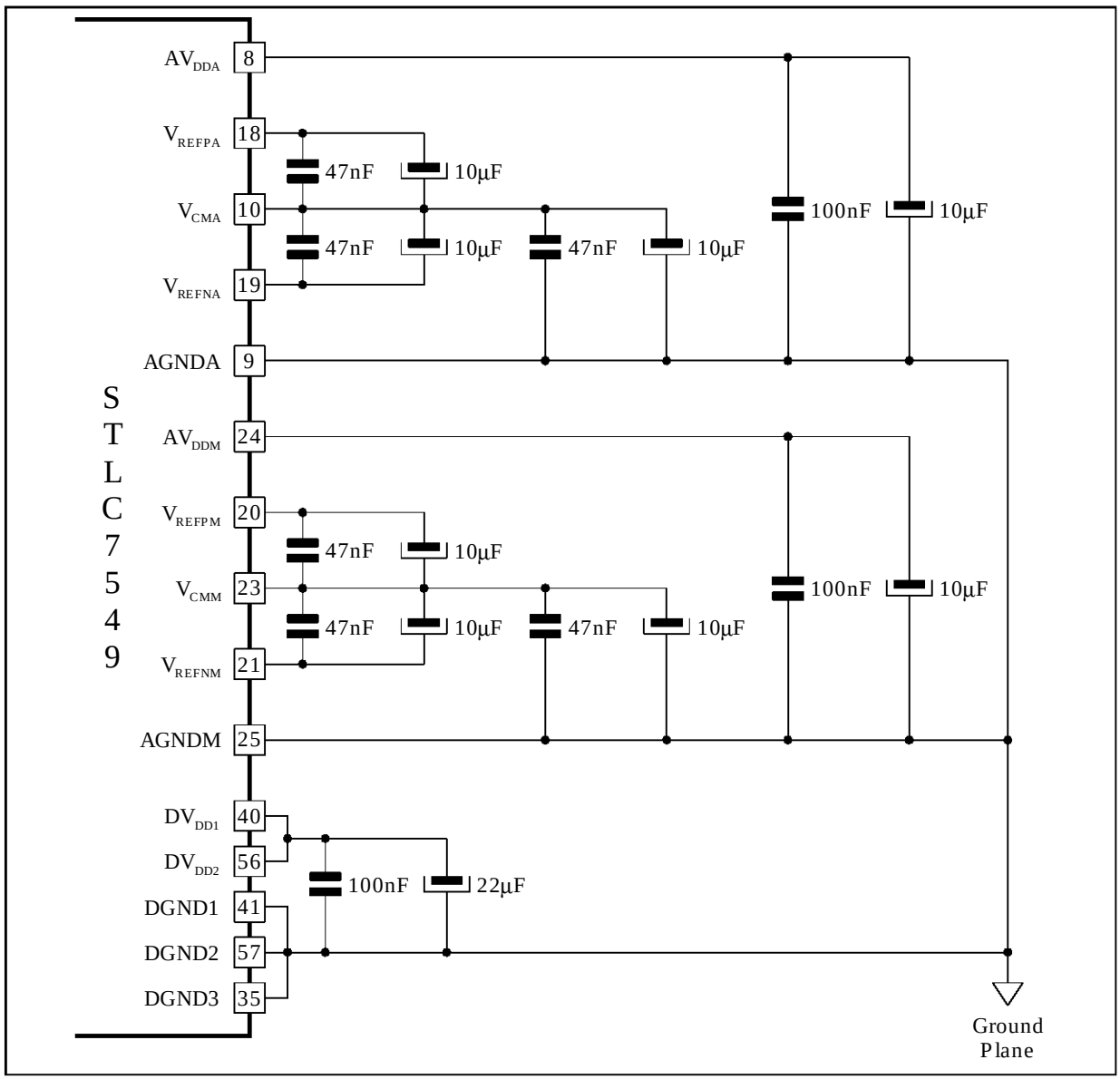
FUNCTIONAL DESCRIPTION (continued)

10 - Voltage Decoupling

To obtain published performance , the analog AV_{DD}, digital DV_{DD} and common mode voltage VCMM (VCMA) should be decoupled with respect to AGND for AV_{DD} and VCMM(VCMA) and to DGND for DV_{DD}. The decoupling is intented to isolate digital noise from the analog section. Decoupling capacitors should be as close as possible to the voltage pin.

All the ground pins must be tied together (see following schematics).

Figure 11



ELECTRICAL SPECIFICATION

Unless otherwise noted, Electrical Characteristics are specified over the operating range.
Typical values are given for V_{DD} = +5V, T_{amb} = 25°C and for nominal master clocks frequency MCLKA = 11.2896MHz and MCLKM = 2.4576MHz.

ABSOLUTE MAXIMUM RATINGS (AGND = DGND = 0V, all voltages with respect to 0V)

Symbol	Parameter	Value	Unit
AV_{DD}	Analog Power Supply	-0.3, 6.0	V
DV_{DD}	Digital Power Supply	-0.3, 6.0	V
I_I	Input Current per Pin (except supply pins)	-10, 10	mA
I_O	Output Current per Pin (except supply pins)	±20	mA
V_{IA}	Analog Input Voltage	-0.3, AV_{DD} + 0.3	V
V_{ID}	Digital Input Voltage	-0.3, DV_{DD} + 0.3	V
V_{IDGPIO}	Digital Input Voltage at GPI/O	5.25	V
T_{oper}	Operating Temperature	0, +70	°C
T_{stg}	Storage Temperature	-40, +125	°C
P_{DMAX}	Maximum Power Dissipation	1500	mW

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Warning : Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND = DGND = 0V, all voltages with respect to 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SINGLE POWER SUPPLY (DV_{DD} = AV_{DD})					
V_{DD}	Supply Voltage	4.75	5	5.25	V
I_D	Digital Supply Current		95		mA
I_A	Analog Supply Current		55		mA
I_{LPH}	Supply Current in Low Power Hardware Mode (PDWN = ”0”) (MCLKs stops)		10		µA
I_{LPSW1}	Supply Current in Low Power Software Mode 1 (see Register 20)		TBD		µA
I_{LPSW2}	Supply Current in Low Power Software Mode 2		TBD		µA
I_{LPSW3}	Supply Current in Low Power Software Mode 3		TBD		µA
P_D	Power Dissipation		750		mW
V_{CM}	Common Mode Voltage Output	AV_{DD}/2 -5%	AV_{DD}/2	AV_{DD}/2 +5%	V
DUAL POWER SUPPLY (DV_{DD} # AV_{DD})					
DV_{DD}	Digital Supply Voltage	3.15	3.3	3.45	V
I_D	Digital Supply Current		50		mA
AV_{DD}	Analog Supply Voltage	4.75	5.0	5.25	V
I_A	Analog Supply Current		55		mA
I_{LPH}	Supply Current in Low Power Hardware Mode (PDWN = ”0”) (MCLKs stops)		TBD		µA
I_{LPSW1}	Supply Current in Low Power Software Mode 1 (see Register 20)		TBD		µA
I_{LPSW2}	Supply Current in Low Power Software Mode 2		TBD		µA
I_{LPSW3}	Supply Current in Low Power Software Mode 3		TBD		µA
P_D	Power Dissipation		450		mW
V_{CM}	Common Mode Voltage Output	AV_{DD}/2 -5%	AV_{DD}/2	AV_{DD}/2 +5%	V
I_{CM}	Common Mode Current Output (see Note 1)		100		µA

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Note 1 : DC current only IF dynamic loading exists, than the common mode voltage output must be buffered or the performance of ADCs and DACs will be degraded

ELECTRICAL SPECIFICATION (continued)

AUDIO

AV_{DD} = 5V, DV_{DD} = 3.3V ; Input levels : Logic 0 = 0V, Logic 1 = DV_{DD} ;
1kHz input sine wave ; Conversion rate = 44.1kHz ;
Measurement bandwidth is 20Hz to 20kHz, 16-bit linear coding for audio, microphone inputs.
Gain setting and Attenuation (0dB) ; 0dBr = $1V_{RMS}$ (sine wave) ; Load impedance 10kΩ, 20pF ;
Unless otherwise specified.

Analog Input Characteristics

Symbol	Parameter		Min.	Typ.	Max.	Unit
ADR	ADC Resolution		16			Bits
DNL	ADC Differential Nonlinearity (see Note 1)		-0.9		+0.9	LSB
SID	Signal to Intermodulation Distortion			85		dB
IcI	Interchannel Isolation (f = 1kHz, V_{input} = 200mV_{PP})		85			dB
IcGM	Interchannel Gain Mismatch	Line Inputs Microphone Inputs	-0.5 -0.5		+0.5 +0.5	dB dB
PIGS	Programmable Input Gain Span	Line Inputs Microphone Inputs	28 55.5	30 57.5	32 59.5	dB dB
GSEr	Gain Step Size Error (see Note 3)	Line Inputs Microphone Inputs			0.5 0.5	dB dB
OFFr	ADC Offset Error (microphone pre-amplifier at maximum gain)	Line Inputs Microphone Inputs		10 600	100 1000	LSB LSB
FSI	Full Scale Input Voltage	Line and Microphone Inputs	2.8	2.9	3.0	V_{PP}
R_{IN}	Input Resistance (see Note 1)	Line Inputs Microphone Inputs	100 10			kΩ kΩ
C_{IN}	Input Capacitance (see Note 1)				15	pF
SNDR	Signal / Noise + Distortion at -6dBr ; 1kHz	ADC Audio ADC Micro	79 70			dB dB
DR	Dynamic Range (see Note 2)		85			dB

7549-07.TBL

Analog Output Characteristics

Symbol	Parameter		Min.	Typ.	Max.	Unit
DAR	DAC Resolution		16			Bits
DNL	DAC Differential Nonlinearity (see Note 1)		-0.9		+0.9	LSB
SNDR	Signal / Noise + Distortion at -10dBr		75			dB
DR	Dynamic Range (see Note 2)		85			dB
SID	Signal to Intermodulation Distortion			85		dB
IcI	Interchannel Isolation	Line Out	85			dB
IcGM	Interchannel Gain Mismatch	Line Out	-0.5	0.1	+0.5	dB
PAS	DAC Programmable Attenuation Span		42	45	48	dB
ASS	DAC Attenuation Step Size		2.5	3	3.5	dB
VOFF	DAC Offset Voltage		-100		+100	mV
FSO	Full Scale Output Voltage		2.8	2.9	3.0	V_{PP}
R_L	Load Resistance		10			kΩ
C_L	Load Capacitance				20	pF
R_{OUT}	Output Resistance				20	Ω
MAtt	Mute Attenuation (0dB gain)		85			dB
OBE	Total Out-of-band Energy (see Note 1)	Fs/2 to 100kHz			-45	dBr

7549-08.TBL

Notes : 1. This specification is guaranteed by characterization, not production testing.
2. DR measured over the full bandwidth 0Hz to FSA/2 with -20dBr signal extrapoled to full scale.
3. The gain step size error is the deviation of a gain or attenuation step from a straight line passing through the no-gain/attenuation value and the ideal full-gain/attenuation value.

ELECTRICAL SPECIFICATION (continued)

MODEM AND TELEPHONY

AV_{DD} = 5V, DV_{DD} = 3.3V ; Input levels : Logic 0 = 0V, Logic 1 = DV_{DD} ; 1kHz input sine wave ; Conversion rate = 9.6kHz. Measurement bandwidth is 100Hz to 4800Hz, 16-bit linear coding for modem inputs and 16-bit linear coding for telephony inputs. For quadraphonic mode the measurement are done with MCLKA = 11.2896MHz and MAMbit set to 1 in Register 20. Gain settings and attenuation (0dB) ; 0dBr = 2 x V_{REFM} peak-to-peak ; Load impedance 10kΩ, 20pF ; unless otherwise specified.

Analog Input Characteristics

Symbol	Parameter		Min.	Typ.	Max.	Unit
ADR	ADC Resolution	Modem #1 Modem #2	16 16			Bits Bits
DNL	ADC Differential Nonlinearity (see Note 1)		-0.9		+0.9	LSB
SID	Signal to Intermodulation Distortion			85		dB
IcI	Interchannel Isolation (f = 1kHz, V_{input} = 200mV_{PP})		85			dB
PIGS	Programmable Input Gain Span	Modem #1 Modem #2		6 12		dB dB
GSEr	Gain Step Size Error (see Note 3)				0.5	dB
OFFr	ADC Offset Error	Modem #1 Modem #2		10 10	100 100	LSB LSB
V_{REFM}	Differential Reference Voltage Output = V_{REFPM} - V_{REFNM}		2.4	2.5	2.6	V
FSI	Full Scale Input Voltage	Modem #1 (differential) Modem #2 (single-ended)		2 x V_{REFM} V_{REFM}		V V
R_{IN}	Input Resistance	Modem #1 Modem #2	100 100			kΩ kΩ
C_{IN}	Input Capacitance			15		pF
SNDR	Signal / Noise + Distorsion at -6dBr ; 1kHz	Modem #1 Modem #2 Quadraphonic Mode		84 79 70		dB dB dB
DR	Dynamic Range (see Note 2)	Modem #1 Modem #2 Quadraphonic Mode		90 85 76		dB dB dB

7549-09.TBL

Notes : 1. This specification is guaranteed by characterization, not production testing.
2. DR measured over the full bandwidth 0Hz to FSA/2 with -20dBr signal extrapoled to full scale.
3. The gain step size error is the deviation of a gain or attenuation step from a straight line passing through the no-gain/attenuation value and the ideal full-gain/attenuation value.

ELECTRICAL SPECIFICATION (continued)

MODEM AND TELEPHONY (continued)

Analog Output Characteristics

Symbol	Parameter		Min.	Typ.	Max.	Unit
DAR	DAC Resolution	Modem #1 Modem #2	16 16			Bits Bits
DNL	DAC Differential Nonlinearity (see Note 1)		-0.9		+0.9	LSB
SNDR	Signal / Noise + Distorsion at -6dBr Signal / Noise + Distorsion at -10dBr	Modem #1 Modem #2 Quadraphonic Mode		84 75 70		dB dB dB
DR	Dynamic Range (see Note 2)	Modem #1 Modem #2 Quadraphonic Mode		90 85 80		dB dB dB
SID	Signal to Intermodulation Distortion			85		dB
IcI	Interchannel Isolation		85			dB
Gabs	Absolute Gain at 1kHz		-0.5	0	+0.5	dB
PAS	DAC Programmable Attenuation Span	Modem #1 Modem #2		6 6		dB dB
VOFF	DAC Offset Voltage		-100		100	mV
FSO	Full Scale Output Voltage	Modem #1 (differential output) Modem #2 (single ended output)		$2 \times V_{REFM}$ V_{REFM}		V V
R_L	Load Resistance		10			kΩ
C_L	Load Capacitance				20	pF
R_{OUT}	Output Resistance				20	Ω
MAtt	Mute Attenuation		85			dB
OBE	Total Out-of-band Energy (see Note 1)	Fs/2 to 100kHz			-45	dBr

7549-10.TBL

Notes : 1. This specification is guaranteed by characterization, not production testing.
2. DR measured over the full bandwidth 0Hz to FSA/2 with -20dBr signal extrapoled to full scale.

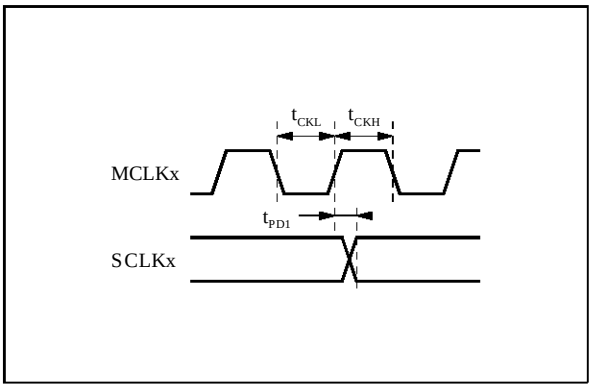
ELECTRICAL SPECIFICATION (continued)

SWITCHING CHARACTERISTICS (AV_{DD} = DV_{DD} = +5V, AGND = DGND = 0V, Outputs loaded with 30pF, Input Levels : Logic 0 = 0V, Logic 1 = DV_{DD})

Symbol	Parameter	Min.	Typ.	Max.	Unit
MCLKA MCLKM	Input Clock (MCLKx) Frequency Modem Mode Quadraphonic Mode	6.144 1.8432	11.2896 2.4576 11.2896	12.288 3.84	MHz MHz MHz
t_{PW}	Master Clock Period		1/MCLKx		-
t_{PW}/t_{CKH} t_{PW}/t_{CKL}	Master Clock (MCLKx) Duty Cycle Pulse Width High Pulse Width Low	20 20		80 80	% %
t_{PD1}	SCLKx Output Delay from MCLKx Rising Edge			35	ns
t_{PD2}	FSYNCx Delay Time			15	ns
t_{S2}	SINx Set-up Time	15			ns
t_{H2}	SINx Hold Time from SCLKx Edge	10			ns
t_{PD3}	SOUTx Delay from SCLKx Edge			25	ns
t_{SCKW1}	SCLK 1 Period		1/(64 x FSA)		s
t_{SCKH1}	SCLK 1 High Time	36			ns
t_{SCKL1}	SCLK 1 Low Time	36			ns
t_{SCKW2}	SCLK 2 Period Modem Mode Quadraphonic Mode		1/(64 x FSM) 1/(64 x FSA)		s s
t_{SCKH2}	SCLK 2 High Time Modem Mode Quadraphonic Mode	1730 36			ns ns
t_{SCKL2}	SCLK 2 Low Time Modem Mode Quadraphonic Mode	1730 36			ns ns
FSA	Audio Sample Frequency (N defined in Reg 20)		MCLKA/ (4 x N x 64)		Hz
FSM	Modem & Telephony Sample Frequency		MCLKM/ (4 x 64)		Hz

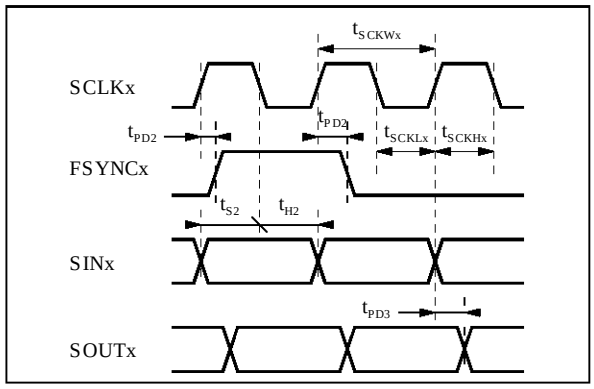
7549-11.TBL

Figure 12 : SCKLx Output Timing



7549-15.EPS

Figure 13



7549-16.EPS

ELECTRICAL SPECIFICATION (continued)

DIGITAL FILTER CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Passband	0		0.4 x Fs	Hz
	Abs Gain at 1kHz	-0.5		+0.5	dB
	Passband Ripple (0 - 0.4 x Fs)	-0.2		+0.2	dB
	Transition Band	0.4 x Fs		0.6 x Fs	Hz
	Stop Band	0.6 x Fs			Hz
	Stop Band Rejection	65			dB

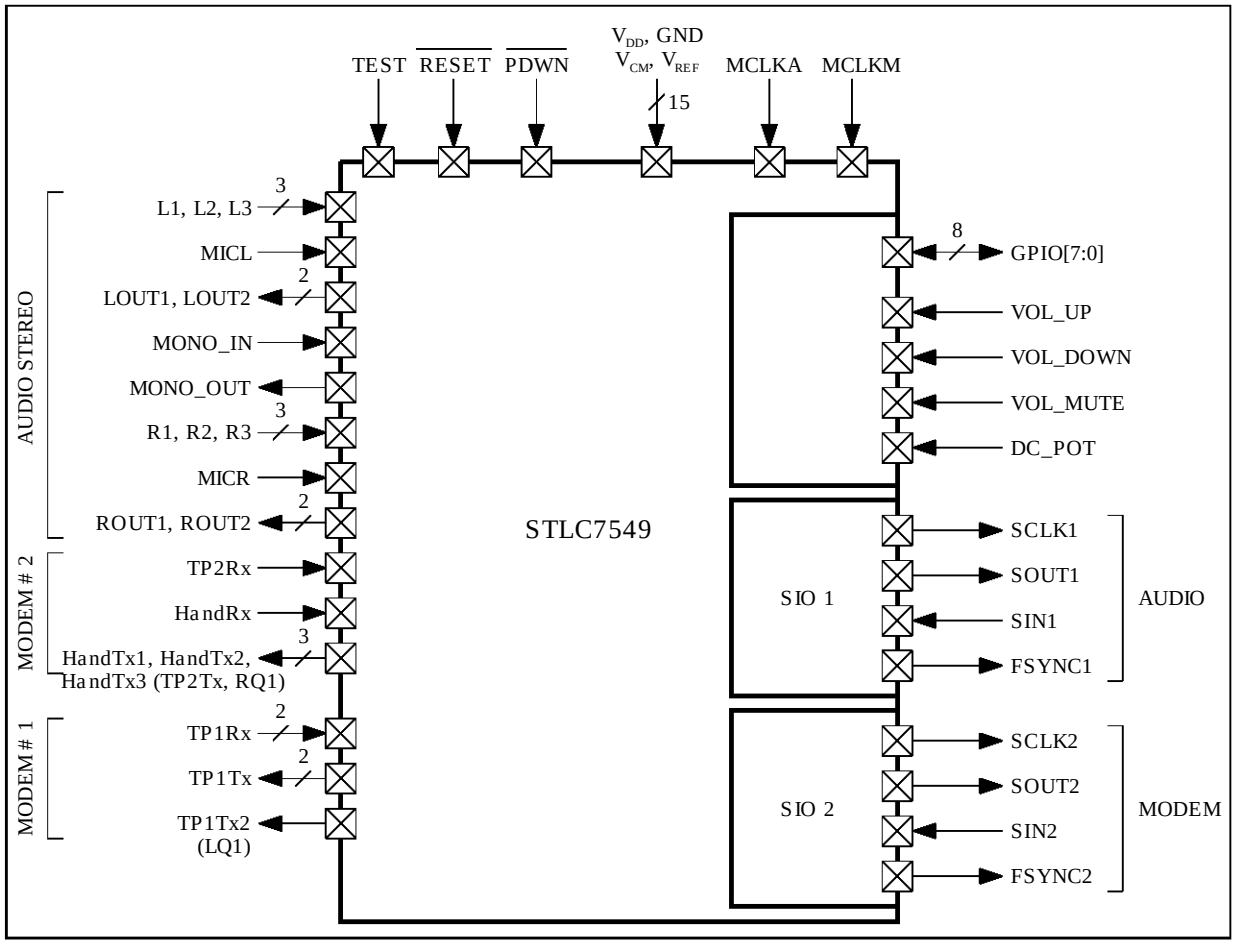
7549-12.TBL

DIGITAL CHARACTERISTICS (AV_{DD} = DV_{DD} = +5V ; AGND = DGND = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage Digital Inputs	2.2		V_{DD} + 0.3	V
V_{IL}	Low level Input Voltage	-0.3		0.8	V
V_{OH}	High Level Output Voltage I_0 = -1mA	2.4		V_{DD}	V
V_{OL}	Low Level Output Voltage I_0 = 1mA			0.4	V
	Input Leakage Current Digital Inputs	-10	±1	10	µA
I_{OL}	Low Level Output Current (GPIO [0:7])			2	mA

7549-13.TBL

INPUT/OUTPUT DESCRIPTION

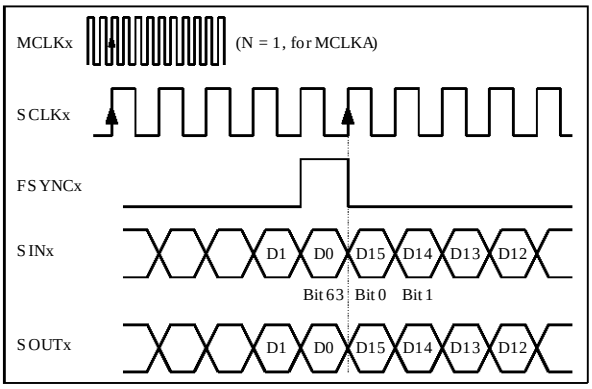


7549-17.EPS

SERIAL INTERFACE

Serial Interface Operation

Figure 14 : Serial Interface Timing



Serial data input is initiated by a frame synchro signal (FSYNC). The data is clocked from SIN into the input shift register (ISR) on the falling edge of SCLK and transfered to the input buffer register (IBR) when a complete 16-bit word has been received, the register is loaded 8 bits clocks later. Data is assumed to be received MSB first.

Serial data output is initiated by a frame synchro signal (FSYNC). The 16-bit data word is loaded into the output shift register (OSR) and serially clocked out of OSR to SOUT on the rising edge of SCLK.

The data/index register of SOUT1 refer to the index register set of SIN1 within the same frame.

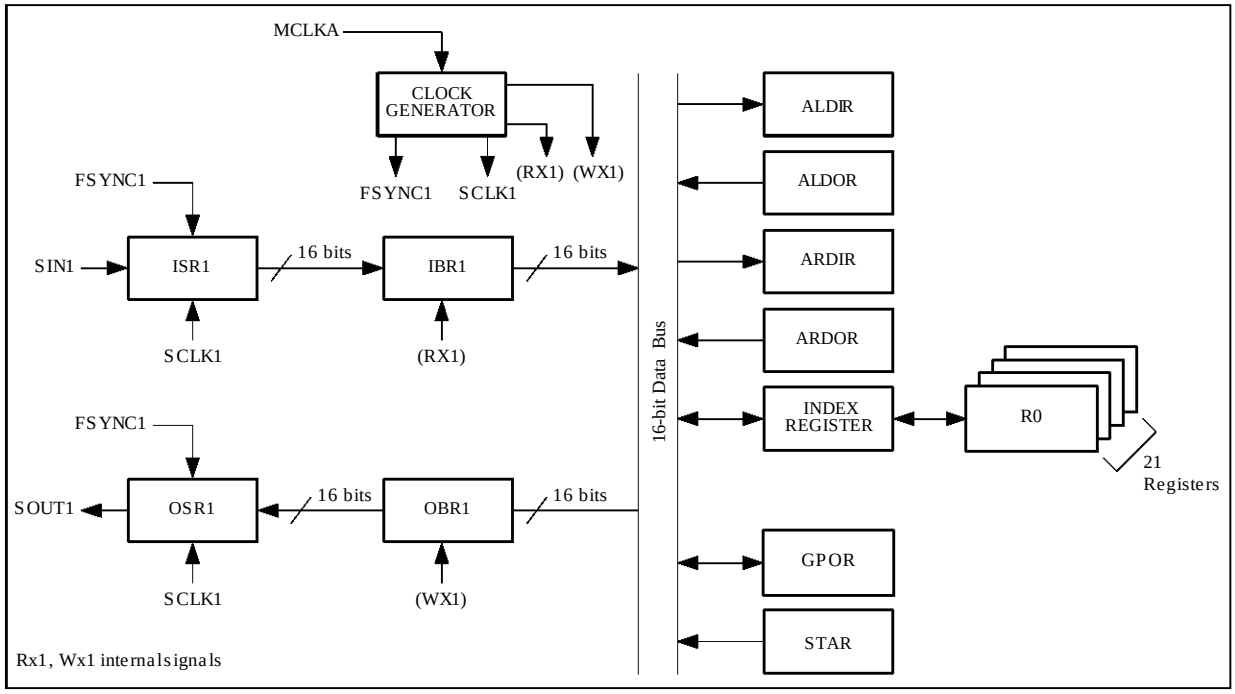
The SCLK is 64 times FSYNC. This mean that the frame contains four slots of 16 bits. The time slots used for circuit function are indicated on the next paragraph.

Serial port 1 and 2
- Frame Synchronization Output (FSYNC)
- Serial Bit Clock Output (SCLK)
- Input Serial Register (ISR)
- Input Buffer Register (IBR)
- Serial Input Data (SIN)
- Output Buffer Register
- Output Serial Register (OSR)

Audio Serial Interface One (Figures 15 and 16)
- Audio Left Data Input Register (ALDIR)
- Audio Left Data Output Register (ALDOR)
- Audio Right Data Input Register (ARDIR)
- Audio Right Data Output Register (ARDOR)
- Index Register (R0 to R20)
- General Purpose Output Register (GPOR)
- Status Audio Register

Modem and Telephone Serial Interface Two
(Figures 17 and 18)
- Modem Data Input Register (MDIR)
- Modem Data Output Register (MDOR)
- Telephone Data Input Register (TDIR)
- Telephone Data Output Register (TDOR)

Figure 15 : Audio Serial Interface Block Diagram



SERIAL INTERFACE (continued)

Figure 16 : Audio Codec Serial Interface (SIO 1) Timing

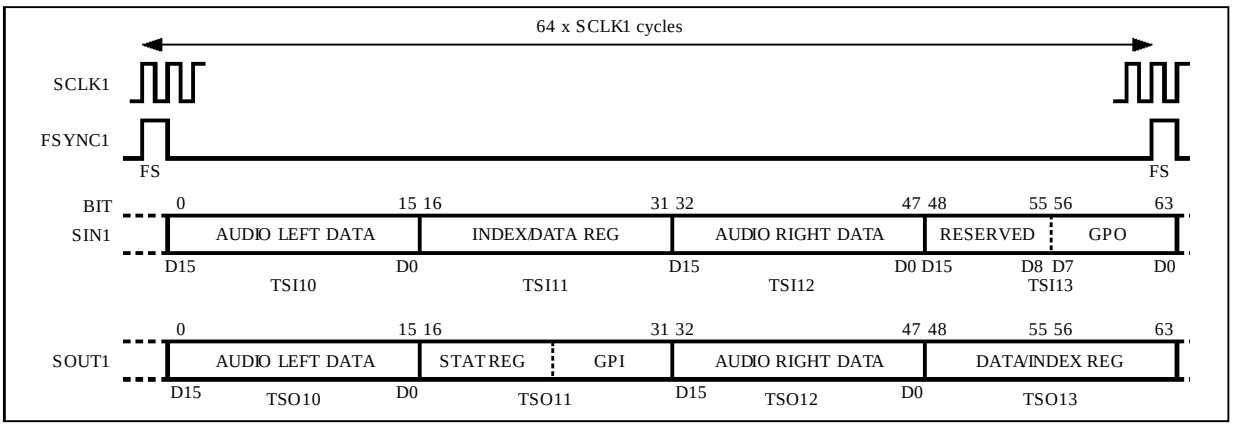


Figure 17 : Modem and Telephone Serial Interface Block Diagram

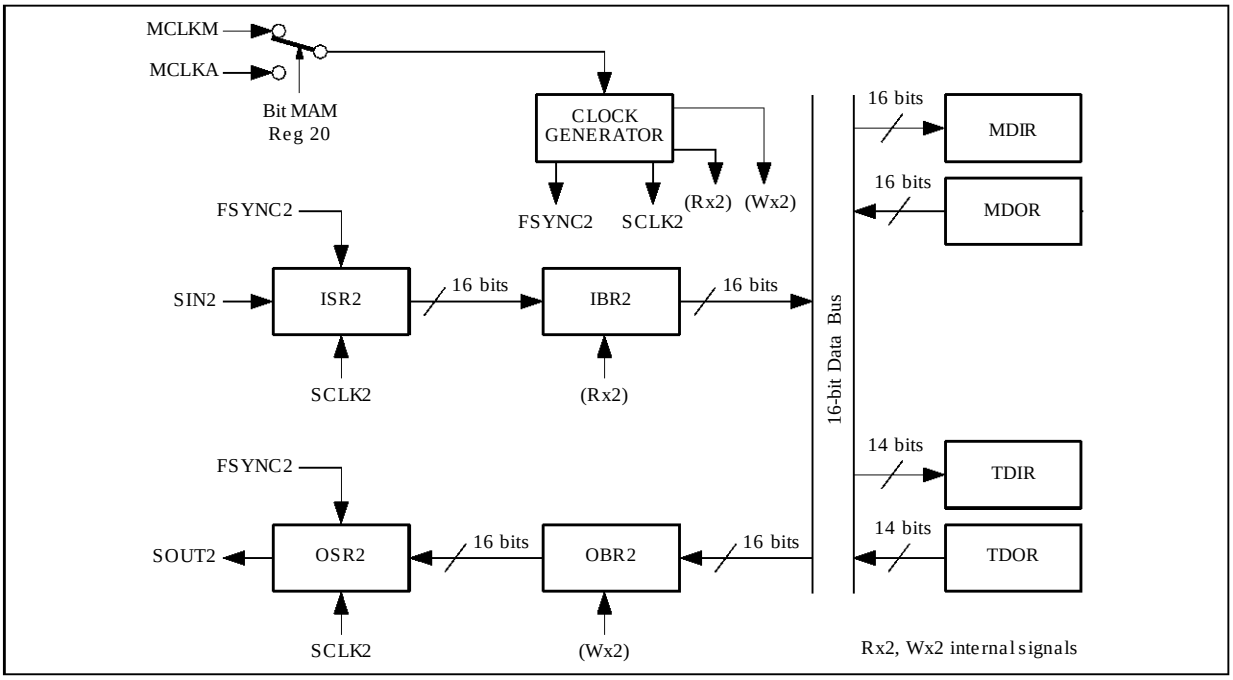
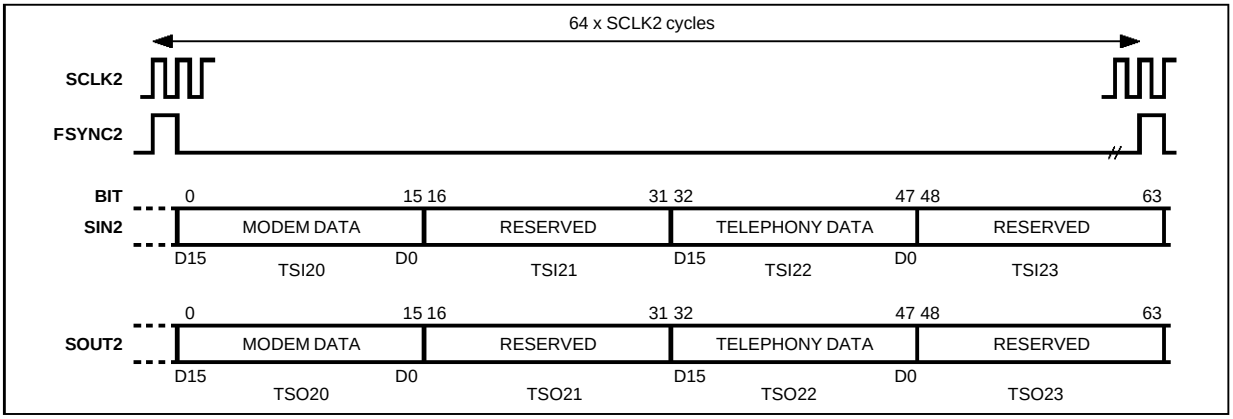


Figure 18 : Modem and Telephony Codecs Serial Interface (SIO 2) Timing



SERIAL INTERFACE BIT DEFINITION

Bit N°	Word N°	Definition

Serial Input #1 Bit Definition (DSP-to-Codec)

0 - 15	0	Audio Left DAC Data (16 bits, MSB first)
16	1	If = "1", write index register set. If = "0", no write , just read index register set
17		Reserved
18		Reserved
19 - 23		Index Register Address (5 bits, MSB first)
24 - 31		Index Register Data (8 bits, MSB first)
32 - 47	2	Audio Right DAC Data (16 bits, MSB first)
48 - 55	3	Reserved
56 - 63		GPIO Output Data [7:0] (8 bits, MSB first). These bits are sent to the pins GPIO [7:0] if their respective configuration bits (CFGPIO [7] thru CFGPIO[0]) are set to the OUTPUT state. Refer to the GPIO configuration register (index Reg # 18) for more information.

Serial Output #1 Bit Definition (Codec-to-DSP)

0 - 15	0	Audio Left ADC Data (16 bits, MSB first)
16	1	+ Mono Codec #2 ADC Overflow (indicates saturation of ADC)
17		+ Mono Codec #1 ADC Overflow (indicates saturation of ADC)
18		+ ADC Left Overflow (indicates saturation of ADC)
19		+ ADC Right Overflow (indicates saturation of ADC)
20		Reserved
21		The Inverted Digital Status Value of Input Pin $\overline{\text{VOL\_MUTE}}$
22		The Inverted Digital Status Value of Input Pin $\overline{\text{VOL\_UP}}$
23		The Inverted Digital Status Value of Input Pin $\overline{\text{VOL\_DOWN}}$
24 - 31		Codec Pins GPIO[7:0] Status (8 bits, MSB first). These bits are a reflection of the digital values on pins GPIO[7:0]. If the GPIO Pin is configured as an OUTPUT, the current setting of that OUTPUT bit will be returned in these status bits. If the GPIO is set to be an INPUT, the digital value on the GPIO input Pin will be read. Refer to the GPIO configuration register (index register 18) for more information.
32 - 47	2	Audio Right ADC Data (16 bits, MSB first)
48 - 50	3	Reserved
51 - 55		Index Register Address Returned (5 bits, MSB first)
56 - 63		Index Register Data Return (8 bits, MSB first)

Serial Input #2 Bit Definition (DSP-to-Codec)

0 - 15	0	Mono Codec #1 DAC Data (16 bits, MSB first)
16 - 31	1	Reserved
32 - 47	2	Mono Codec #2 DAC Data (16 bits, MSB first)
48 - 63	3	Reserved

Serial Output #2 Bit Definition (Codec-to-DSP)

0 - 15	0	Mono Codec #1 ADC Data (16 bits, MSB first)
16 - 31	1	Reserved
32 - 47	2	Mono Codec #2 ADC Data (16 bits, MSB first)
48 - 63	3	Reserved

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REGISTER DESCRIPTION

Index Register Map

Register	Name
0	Identification Register
1	Line Input #1 Gain Control
2	Line Input #2 Gain Control
3	Line Input #3 Gain Control
4	Right Microphone Input Gain Control
5	Left Microphone Input Gain Control
6	Right Channel Audio ADC Summer Control
7	Left Channel Audio ADC Summer Control
8	Right Channel Audio DAC Summer Control
9	Left Channel Audio DAC Summer Control
10	Audio Line Output Attenuators
11	Audio Output Mute Control
12	Mono Input/Output Control
13	Mono Codec #1 Input Control
14	Mono Codec #1 Output Control
15	Mono Codec #2 Input Control
16	Mono Codec #2 Output Control
17	ADC/DAC Loopback Control Register
18	GPIO Configuration Register
19	Digital Control Register #1
20	Digital Control Register #2
21	Saturation Clear Register

Index Register 0 : Identification Register

7	6	5	4	3	2	1	0
Chip Identification				Revision Code			

Read only register. 0001-0001

Index Register 1 : Line Input #1 Gain Control Register

7	6	5	4	3	2	1	0
LI1G3	LI1G2	LI1G1	LI1G0	RI1G3	RI1G2	RI1G1	RI1G0

RI1G3 to RI1G0 : Reset value : 0000.
Right line input #1 gain select.

LI1G3 to LI1G0 : Reset value : 0000.
Left line input #1 gain select.

Refer to the line input gain select table (Table 1) to understand how these bits relate to the actual gain/attenuation value.

Index Register 2 : Line Input #2 Gain Control Register

7	6	5	4	3	2	1	0
LI2G3	LI2G2	LI2G1	LI2G0	RI2G3	RI2G2	RI2G1	RI2G0

RI2G3 to RI2G0 : Reset value : 0000.
Right line input #2 gain select.

LI2G3 to LI2G0 : Reset value : 0000.
Left line input #2 gain select.

Refer to the line input gain select table (Table 1) to understand how these bits relate to the actual gain/attenuation value.

REGISTER DESCRIPTION (continued)

Index Register 3 : Line Input #3 Gain Control Register

7	6	5	4	3	2	1	0
LI3G3	LI3G2	LI3G1	LI3G0	RI3G3	RI3G2	RI3G1	RI3G0

RI3G3 to RI3G0 : Reset value : 0000.
Right line input #3 gain select.

LI3G3 to LI3G0 : Reset value : 0000.
Left line input #3 gain select.

Refer to the line input gain select table (Table 1) to understand how these bits relate to the actual gain/attenuation value.

Table 1 : Line Input Gain Select (G1)

Bit Code	Decimal	Gain (dB)	Bit Code	Decimal	Gain (dB)
0000	0	-24	1000	8	-8
0001	1	-22	1001	9	-6
0010	2	-20	1010	10	-4
0011	3	-18	1011	11	-2
0100	4	-16	1100	12	+0
0101	5	-14	1101	13	+2
0110	6	-12	1110	14	+4
0111	7	-10	1111	15	+6

Index Register 4 : Right Microphone Input Gain Control Register

7	6	5	4	3	2	1	0
			+MPRER	RIMG3	RIMG2	RIMG1	RIMG0

RIMG3 to RIMG0 : Reset value : 0000.
Right input microphone gain select.
Refer to the microphone gain table (Table 2) to understand how these bits relate to the actual gain/attenuation value.

+MPRER : Reset value : 0
Setting this bit to a 1 will place a +20dB pre-amplifier in the microphone left signal path. If this bit is a 0, the pre-amplifier gain will be +0dB (see Table 3).

Index Register 5 : Left Microphone Input Gain Control Register

7	6	5	4	3	2	1	0
			+MPREL	LIMG3	LIMG2	LIMG1	LIMG0

LIMG3 to LIMG0 : Reset value : 0000.
Left input microphone gain select.
Refer to the microphone gain table (Table 2) to understand how these bits relate to the actual gain/attenuation value.

+MPREL : Reset value : 0.
Setting this bit to a 1 will place a +20dB pre-amplifier in the microphone left signal path. If this bit is a 0, the gain will be +0dB.

Table 2 : Microphone Gain Select (G2)

Bit Code	Decimal	Gain (dB)	Gain with +20dB preamp. (dB)	Bit Code	Decimal	Gain (dB)	Gain with +20dB preamp. (dB)
0000	0	+0.0	+20.0	1000	8	+20.0	+40.0
0001	1	+2.5	+22.5	1001	9	+22.5	+42.5
0010	2	+5.0	+25.0	1010	10	+25.0	+45.0
0011	3	+7.5	+27.5	1011	11	+27.5	+47.5
0100	4	+10.0	+30.0	1100	12	+30.0	+50.0
0101	5	+12.5	+32.5	1101	13	+32.5	+52.5
0110	6	+15.0	+35.0	1110	14	+35.0	+55.0
0111	7	+17.5	+37.5	1111	15	+37.5	+57.5

Table 3 : Pre-amplifier (P)

MPRER / MPREL	Pre-amplifier Gain (P)
0	+0dB
1	+20dB

REGISTER DESCRIPTION (continued)

Index Register 6 : Right ADC Summer Control

7	6	5	4	3	2	1	0
		-MUTRAD	-MUTRAP	-MUTRAM	-MUTRA3	-MUTRA2	-MUTRA1

-MUTRA1 : Reset value : 0. Mute right line input #1 of the ADC right summer. Setting this bit to 0 mutes the signal.

-MUTRA2 : Reset value : 0. Mute right line input #2 of the ADC right summer. Setting this bit to 0 mutes the signal.

-MUTRA3 : Reset value : 0. Mute right line input #3 of the ADC right summer. Setting this bit to 0 mutes the signal.

-MUTRAM : Reset value : 0. Mute right microphone input of the ADC right summer. Setting this bit to 0 mutes the signal.

-MUTRAP : Reset value : 0. Mute mono input of the ADC right summer. Setting this bit to 0 mutes the signal.

-MUTRAD : Reset value : 0. Mute right DAC signal into the ADC right summer. This signal is the right DAC output of the codec wrapped back around into the ADC input summer. Setting this bit to 0 mutes the signal.

Index Register 7 : Left ADC Summer Control

7	6	5	4	3	2	1	0
		-MUTLAD	-MUTLAP	-MUTLAM	-MUTLA3	-MUTLA2	-MUTLA1

-MUTLA1 : Reset value : 0. Mute left line input #1 of the ADC left summer. Setting this bit to 0 mutes the signal.

-MUTLA2 : Reset value : 0. Mute left line input #2 of the ADC left summer. Setting this bit to 0 mutes the signal.

-MUTLA3 : Reset value : 0. Mute left line input #3 of the ADC left summer. Setting this bit to 0 mutes the signal.

-MUTLAM : Reset value : 0. Mute left microphone input of the ADC left summer. Setting this bit to 0 mutes the signal.

-MUTLAP : Reset value : 0. Mute mono input of the ADC left summer. Setting this bit to 0 mutes the signal.

-MUTLAD : Reset value : 0. Mute left DAC signal into the ADC left summer. This signal is the left DAC output of the codec wrapped back around into the ADC input summer. Setting this bit to 0 mutes the signal.

Index Register 8 : Right DAC Summer Control

7	6	5	4	3	2	1	0
		-MUTRDD	-MUTRDP	-MUTRDM	-MUTRD3	-MUTRD2	-MUTRD1

-MUTRD1 : Reset value : 0. Mute right line input #1 of the DAC right summer. Setting this bit to 0 mutes the signal.

-MUTRD2 : Reset value : 0. Mute right line input #2 of the DAC right summer. Setting this bit to 0 mutes the signal.

-MUTRD3 : Reset value : 0. Mute right line input #3 of the DAC right summer. Setting this bit to 0 mutes the signal.

-MUTRDM: Reset value : 0. Mute right microphone input of the DAC right summer. Setting this bit to 0 mutes the signal.

-MUTRDP : Reset value : 0. Mute mono input of the DAC right summer. Setting this bit to 0 mutes the signal.

-MUTRDD : Reset value : 0. Mute right DAC signal going into the DAC right summer. This input is the main right DAC output of the sigma-delta codec. Setting this bit to 0 mutes the signal.

REGISTER DESCRIPTION (continued)

Index Register 9 : Left DAC Summer Control

7	6	5	4	3	2	1	0
		-MUTLDD	-MUTLDP	-MUTLDM	-MUTLD3	-MUTLD2	-MUTLD1

-MUTLD1 : Reset value : 0. Mute left line input #1 of the DAC left summer. Setting this bit to 0 mutes the signal.

-MUTLD2 : Reset value : 0. Mute left line input #2 of the DAC left summer. Setting this bit to 0 mutes the signal.

-MUTLD3 : Reset value : 0. Mute left line input #3 of the DAC left summer. Setting this bit to 0 mutes the signal.

-MUTLDM : Reset value : 0. Mute left microphone input of the DAC left summer. Setting this bit to 0 mutes the signal.

-MUTLDP : Reset value : 0. Mute mono input of the DAC left summer. Setting this bit to 0 mutes the signal.

-MUTLDD : Reset value : 0. Mute left DAC signal into the DAC left summer. This input is the main left DAC output of the sigma-delta codec. Setting this bit to 0 mutes the signal.

Index Register 10 : Audio Line Output Attenuator Control

7	6	5	4	3	2	1	0
LOUTG3	LOUTG2	LOUTG1	LOUTG0	ROUTG3	ROUTG2	ROUTG1	ROUTG0

ROUTG3 to ROUTG0 : Reset value : 0000. Right line output gain select.

LOUTG3 to LOUTG0 : Reset value : 0000. Left line output gain select.

Refer to the line output attenuator select Table (Table 4) to understand how these bits relate to the actual attenuation value.

Table 4 : Line Output Attenuator Select (A1)

Bit Code	Decimal	Gain (dB)	Bit Code	Decimal	Gain (dB)
0000	0	0	1000	8	-24
0001	1	-3	1001	9	-27
0010	2	-6	1010	10	-30
0011	3	-9	1011	11	-33
0100	4	-12	1100	12	-36
0101	5	-15	1101	13	-39
0110	6	-18	1110	14	-42
0111	7	-21	1111	15	-45

Index Register 11 : Audio Output Mute Control

7	6	5	4	3	2	1	0
			-MUTEX	-MUTL2	-MUTL1	-MUTR2	-MUTR1

-MUTR1 : Reset value : 0. Mute right line output #1. Setting this bit to 0 mutes the output Pin ROUT1.

-MUTR2 : Reset value : 0. Mute right line output #2. Setting this bit to 0 mutes the output Pin ROUT2.

-MUTL1 : Reset value : 0. Mute left line output #1. Setting this bit to 0 mutes the output Pin LOUT1.

-MUTL2 : Reset value : 0. Mute left line output #2. Setting this bit to 0 mutes the output Pin LOUT2.

-MUTEX : Reset value : 1 (unmute). This bit is read only and is the output of toggle/untoggled debounced external mute.

Index Register 12 : Mono Input/Output Control

7	6	5	4	3	2	1	0
			-MUTPCP	-MUTPCR	-MUTPCL	PGAIN1	PGAIN0

PGAIN1, PGAIN0 : Reset value : 01. Mono input attenuator select (A4). These two bits select the input attenuation value as shown in the Table 5.

-MUTPCL : Reset value : 0. Mute DAC left into mono output summer. Setting this bit to 0 mutes the signal.

-MUTPCR : Reset value : 0. Mute DAC right into mono output summer. Setting this bit to 0 mutes the signal.

-MUTPCP : Reset value : 1. Mute mono input into mono output summer. This bit will power on to a one (1) so that the PC system "beeper" sounds coming into the mono input pin will be looped to the mono output pin so that PC system sounds can be heard during power-up. Setting this bit to 0 mutes this loop path.

Table 5 : Mono Input Attenuator

PGAIN1	PGAIN0	Gain (A4)
0	0	0dB
0	**1**	**-10dB**
1	0	-20dB
1	1	-30dB

REGISTER DESCRIPTION (continued)

Index Register 13 : Modem Codec #1 Input Control

7	6	5	4	3	2	1	0
							M1G0

M1G0 : Reset value : 0.
Gain select for mono codec #1 input amplifier (G4) (see Table 6).

Table 6 : Codec #1 Amplifier Gain

M1G0	Amplifier Gain (G4)
0	+0dB
1	+6dB

Note : If single-ended hardware, M1G0 must be set to 1 to +0dB gain.

Index Register 14 : Mono Codec #1 Output Control

7	6	5	4	3	2	1	0
					M1TXG	-M1TX2	-M1TX1

-M1TX1 : Reset value : 0. Setting this bit to 1 will enable the mono codec #1 DAC output to the TP1TX1+/TP1TX1- output Pins. If set to 0, the pins are muted.

-M1TX2 : Reset value : 0. Setting this bit to 1 will enable the mono codec #1 DAC output to the TP1TX2 output Pin. If set to 0, the pin is muted.

M1TXG : Reset value : 0. Setting this bit to 1 will place a -6dB attenuator in the output DAC path. Setting this bit to 0 will result in a gain path of 0dB (A2).

Table 7 : Transmit Gain (A2)

M1TXG	Transmit Amplifier Gain (A2)
0	+0dB
1	-6dB

Index Register 15 : Mono Codec #2 Input Control

7	6	5	4	3	2	1	0
TP2RXG1	TP2RXG0	-M2MICL	-M2MICR	-M2TP2	-M2HRX	HRXG1	HRXG0

TP2RXG1, TP2RXG0 : Reset value : 00.
TP2Rx gain select. These two bits determine the gain of the input amplifier of the TP2RX input Pin of mono codec #2. The Table 8 illustrates the bit definitions of the four possible gain settings. This amplifier is only applied to the TP2RX input of mono codec #2.

HRXG1, HRXG0 : Reset value : 00.
HandRx gain select. These two bits determine the gain of the input amplifier of the HandRx input Pin of mono codec #2. The Table 8 illustrates the bit definitions of the four possible gain settings. This amplifier is only applied to the HandRx input of mono codec #2.

-M2HRX : Reset value : 0.
Setting this bit to 1 will enable the HandRx input into the ADC summer of the mono codec #2. Setting the bit to 0 will mute the signal.

-M2TP2 : Reset value : 0.
Setting this bit to 1 will enable the TP2Rx input into the ADC summer of the mono codec #2. Setting the bit to 0 will mute the signal.

-M2MICR : Reset value : 0.
Setting this bit to 1 will enable the internally amplified microphone right signal into the ADC summer of the mono codec #2. Setting the bit to 0 will mute the signal.

-M2MICL : Reset value : 0.
Setting this bit to 1 will enable the internally amplified microphone left signal into the ADC summer of the mono codec #2. Setting the bit to 0 will mute the signal.

Table 8 : TP2Rx and HANDRx Input Gain (G3)

Bit Code		Gain (G3)
0	0	-4dB
0	1	0dB
1	0	+4dB
1	1	+8dB

REGISTER DESCRIPTION (continued)

Index Register 16 : Modem Codec #2 Output Control

7	6	5	4	3	2	1	0
				M2TXG	-M2TX3	-M2TX2	-M2TX1

-M2TX1 : Reset value : 0. Setting this bit to 1 will enable the mono codec #2 DAC output to the HandTx1 output Pin. Setting the bit to 0 will mute the signal.

-M2TX2 : Reset value : 0. Setting this bit to 1 will enable the mono codec #2 DAC output to the HandTx2 output Pin. Setting the bit to 0 will mute the signal.

-M2TX3 : Reset value : 0. Setting this bit to 1 will enable the mono codec #2 DAC output to the HandTx3 output Pin. Setting the bit to 0 will mute the signal.

M2TXG : Reset value : 0. Setting this bit to 1 will place a -6dB attenuator in the output DAC path. Setting this bit to 0 will result in a gain path of 0dB.

Table 9 : Transmit Gain (A2)

M2TXG	Transmit Amplifier Gain (A2)
0	+0dB
1	-6dB

Index Register 17 : Loopback Control Register

7	6	5	4	3	2	1	0
				+LOOPM2	+LOOPM1	+LOOPL	+LOOPR

+LOOPR : Reset value : 0. Setting this bit to 1 will loop the ADC digital data to the DAC converter on the audio codec right converter. Setting this bit to 0 will cause the DAC converter to receive its digital data from the serial port which is normal operation.

+LOOPL : Reset value : 0. Setting this bit to 1 will loop the ADC digital data to the DAC converter on the audio codec left converter. Setting this bit to 0 will cause the DAC converter to receive its digital data from the serial port which is normal operation.

+LOOPM1 : Reset value : 0. Setting this bit to 1 will loop the ADC digital data to the DAC converter on the mono codec #1 converter. Setting this bit to 0 will cause the DAC converter to receive its digital data from the serial port which is normal operation.

+LOOPM2 : Reset value : 0. Setting this bit to 1 will loop the ADC digital data to the DAC converter on the mono codec #2 converter. Setting this bit to 0 will cause the DAC converter to receive its digital data from the serial port which is normal operation.

Index Register 18 : GPIO Configuration Register

7	6	5	4	3	2	1	0
CFGPIO7	CFGPIO6	CFGPIO5	CFGPIO4	CFGPIO3	CFGPIO2	CFGPIO1	CFGPIO0

CFGPIO0 : Reset value : 0. If this bit is set to 0, then the Pin GPIO0 is an input. If this bit is set to 1, then the Pin is an output.

CFGPIO1 : Reset value : 0. If this bit is set to 0, then the Pin GPIO1 is an input. If this bit is set to 1, then the Pin is an output.

CFGPIO2 : Reset value : 0. If this bit is set to 0, then the Pin GPIO2 is an input. If this bit is set to 1, then the Pin is an output.

CFGPIO3 : Reset value : 0. If this bit is set to 0, then the Pin GPIO3 is an input. If this bit is set to 1, then the Pin is an output.

CFGPIO4 : Reset value : 0. If this bit is set to 0, then the Pin GPIO4 is an input. If this bit is set to 1, then the Pin is an output.

CFGPIO5 : Reset value : 0. If this bit is set to 0, then the Pin GPIO5 is an input. If this bit is set to 1, then the Pin is an output.

CFGPIO6 : Reset value : 0. If this bit is set to 0, then the Pin GPIO6 is an input. If this bit is set to 1, then the Pin is an output.

CFGPIO7 : Reset value : 0. If this bit is set to 0, then the Pin GPIO7 is an input. If this bit is set to 1, then the pin is an output.

REGISTER DESCRIPTION (continued)

Index Register 19 : Digital Control Register #1

7	6	5	4	3	2	1	0
DCVOL3	DCVOL2	DCVOL1	DCVOL0	+DCVOL	+PBVOL	CALIBM	CALIBA

DCVOL3-0 : Read only DC volume control value (see +DCVOL bit for explanation).

+DCVOL : Reset value : 0. + Enable DC volume control circuitry. If the DCVOL bit is enabled, the codec will use a DC voltage range from a potentiometer attached to the external chip pin DC_POT to determine a 4-bit value to be used as the main left/right output attenuator register value. Regardless of the setting of this DCVOL bit, this 4-bit value can be read by DSP software since the 4-bit value is reflected in the Register 19 (bits [7:4]). The DSP software can use this 4-bit value for unique functions. Setting this bit to 1 will enable the circuitry on the codec which permits the external potentiometer to control the main left/right output attenuator register 4-bit value in Register 10.

+PBVOL : Reset value : 0. + Enable pushbutton volume circuitry. Setting this bit to 1 will enable the pushbutton digital volume control input pins to influence the main left/right output attenuator register values in Register 10. The output attenuators have 16 possible states and the VOL_UP and VOL_DOWN input pins will make the attenuator register value increment or decrement from 0 to 15. The VOL_MUTE input pin will affect the main left/right output mute blocks in Register 11. Regardless of the value of this control bit, the three digital input values of the UP, DOWN and MUTE pins are reflected in the STATUS word that is sent to the DSP on the codec SOUT1 line.

CALIBA, CALIBM : Reset value : 0. Setting the bit CALIBA to 1 will force a calibration of all audio converters and the bit CALIBM to 1will force a calibration of all modem converters. The length of time required for calibration is 23ms min. at 44.1kHz (section 4 of the functional description) and after CALIB is automatically reset to 0 when calibration is completed.

Note : If +DCVOL and +PBVOL are set to 1, the priority is given to +DCVOL.

Index Register 20 : Digital Control Register #2

7	6	5	4	3	2	1	0
		MOR	MAM	NDIV1	NDIV0	SWPDN1	SWPDN0

MOR : Reset value : 0. When this bit is set to 0 the mono codecs #1 and #2 are in modem mode otherwise there are quadraphonic mode.

MAM : Reset value :0. Mono codecs #1 and #2 clocks derived from MCLKM when set to 0. If this bit is set to 1, all codecs clocks are issued from MCLKA (quadraphonic mode).

NDIV1, NDIV0 : Reset value : 00. Ratio FSA versus MCLKA : see Table 11. Typical sampling frequency obtained with MCLK = 11.2896MHz : see Table 12.

SWPDN1, SWPDN0 : Reset value : 00. Software power-down mode options. (see Table 13).

Table 10 : Sampling Frequency Setting

Bit 3	Bit 2	N	FSA
0	0	1	24kHz → 48kHz
0	1	2	12kHz → 24kHz
1	0	4	6kHz → 12kHz
1	1	8	3kHz → 6kHz

Table 11 : Typical FSA with MCLKA=11.2896MHz

Bit 3	Bit 2	N	FSA
0	0	1	44.1kHz
0	1	2	22.05kHz
1	0	4	11.025kHz
1	1	8	5.5125kHz

Table 12

Bit 1	Bit 0	Power-down Mode
0	0	SWPDN Mode 0 : all codec circuitry is active.
0	1	SWPDN Mode 1 : Audio left/right ADC/DAC are powered down. Mono codecs #1 and #2 are active. All input and output analog mixers are active. Serial port #1 active. Serial port #2 active.
1	0	SWPDN Mode 2 : Audio left/right ADC/DAC are active. Mono codecs #1 and #2 are powered down. All input and output analog mixers are active. Serial port #1 active. Serial port #2 in-active.
1	1	SWPDN Mode 3 : All codec ADC/DACs are powered down. All input and output analog mixers are active. Serial port #1 active. Serail port #2 in-active.

REGISTER DESCRIPTION (continued)

Index Register 21 : Saturation Clear Register

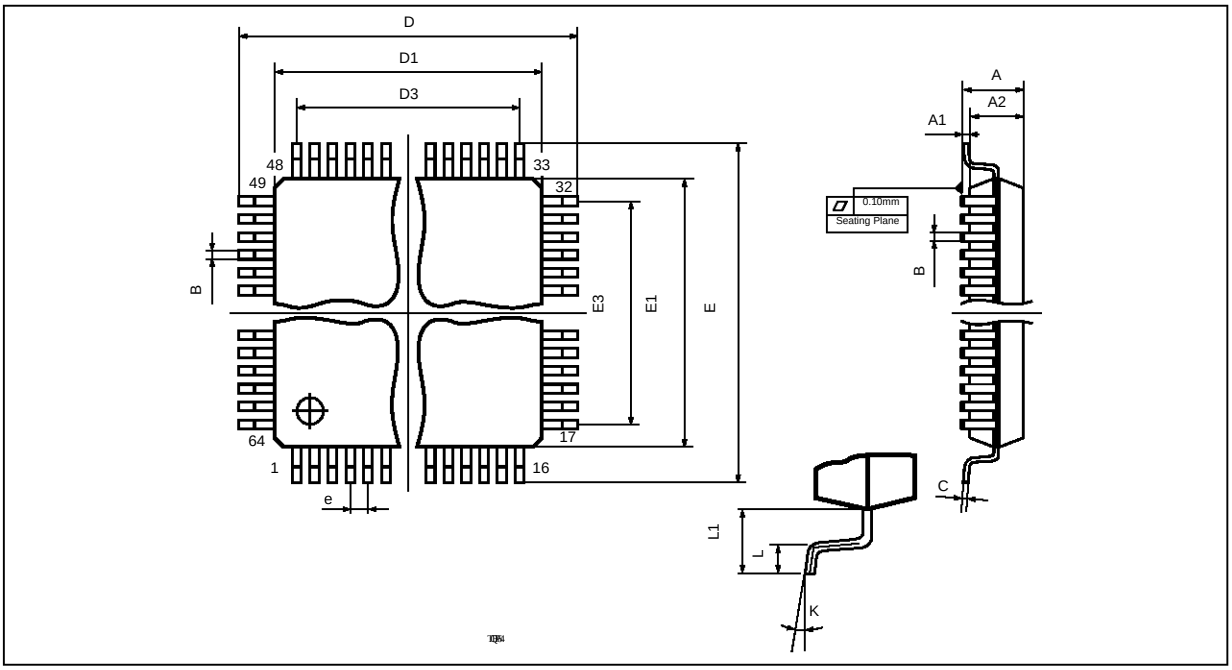
7	6	5	4	3	2	1	0
				ADC MODEM #2	ADC MODEM #1	ADC LEFT	ADC RIGHT

ADC LEFT, ADC RIGHT, ADC MODEM #1, ADC MODEM #2 : Reset value : 0000.

When bit is set to 1, the STLC7549 will clear the respective ADC overflow bit in the serial output datastream periods. This is a write only register.

PACKAGE MECHANICAL DATA

64 PINS - THIN QUAD FLAT PACK (Body 10 x 10 x 1.40mm)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.18	0.23	0.28	0.007	0.009	0.011
C	0.12	0.16	0.20	0.0047	0.0063	0.0079
D		12.00			0.472	
D1		10.00			0.394	
D2		7.50			0.295	
e		0.50			0.0197	
E		12.00			0.472	
E1		10.00			0.394	
E2		7.50			0.295	
F		1.00			0.0393	
K	0^o (min.), 7^o (max.)					
L	0.40	0.60	0.75	0.0157	0.0236	0.0295

TQFP64B.TBL